Subject: cad mid slot 2
From: IKENOYA Katsutoshi <j05002@ie.u-ryukyu.ac.jp>
Date: Sat, 23 Dec 2006 14:23:00 +0900
To: wada@ie.u-ryukyu.ac.jp

・VHDLファイル

```
-wavegen.vhd

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;

entity WAVEGEN is
port (
CLK : in std_logic;
RESET : in std_logic;
OFFSET: in std_logic_vector(2 downto 0); -- <3,3,u>
W_I : out std_logic_vector(9 downto 0); -- <10,0,t>
W_Q : out std_logic_vector(9 downto 0)); -- <10,0,t>
end;

architecture RTL of WAVEGEN is

signal SUM : std_logic_vector(5 downto 0):="000000";
signal ADDR : std_logic_vector(5 downto 0);

begin

process(CLK,RESET)
begin
if(CLK'event and CLK = '1')then
SUM <= signed(OFFSET(2)&OFFSET(2)&OFFSET(2)&OFFSET) + signed(SUM);
if(RESET='1')then
SUM <= "000000";
ADDR <= SUM;
else
ADDR <= SUM;
end if;

end if;
end process;

process (ADDR)
variable iaddr : integer;
variable qaddr : integer;
type rom_type is array(0 to 63) of std_logic_vector(9 downto 0);
constant cos_table : rom_type := (
"0111111111","0111111110","0111110110","0111101010",
"0111011001","0111000100","0110101010","0110001100",
"0101101010","0101000101","0100011100","0011110001",
"0011000100","0010010101","0001100100","0000110010",
"0000000000","1111001110","1110011100","1101101011",
"1100111100","1100001111","1011100100","1010111011",
"1010010110","1001110100","1001010110","1000111100",
"1000100111","1000010110","1000001010","1000000010",
"1000000000","1000000010","1000001010","1000010110",
"1000100111","1000111100","1001010110","1001110100",
"1010010110","1010111011","1011100100","1100001111",
"1100111100","1101101011","1110011100","1111001110",
"0000000000","0000110010","0001100100","0010010101",
"0011000100","0011110001","0100011100","0101000101",
```

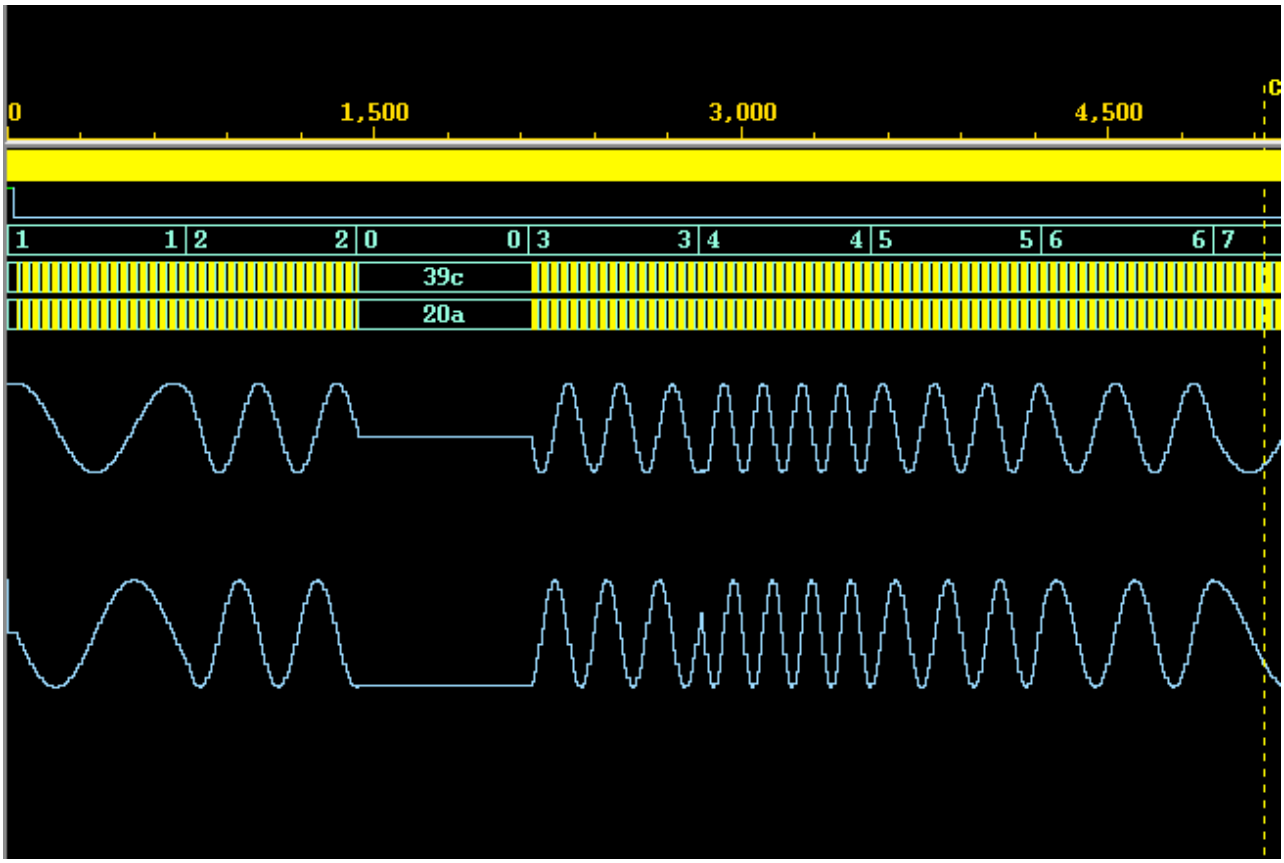
```
"0101101010","0110001100","0110101010","0111000100",
"0111011001","0111101010","0111110110","0111111110"
);

begin
iaddr := conv_integer(unsigned(ADDR));
qaddr := conv_integer(unsigned(ADDR)+16);
W_I <= cos_table(iaddr);
W_Q <= cos_table(qaddr);
end process;

end;
--------------------------------------------------------------------------------------------------------
-test_wavegen2.vhd

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;

entity TESTBENCH_WAVEGEN is
end;

architecture SIM_DATA of TESTBENCH_WAVEGEN is

component WAVEGEN
port (
CLK : in std_logic;
RESET : in std_logic;
OFFSET: in std_logic_vector(2 downto 0); -- <3,3,u>
W_I : out std_logic_vector(9 downto 0); -- <10,0,t>
W_Q : out std_logic_vector(9 downto 0)); -- <10,0,t>
end component;

signal CLK : std_logic := '0' ;
signal RESET : std_logic := '1' ; -- RESET STATE
signal OFFSET : std_logic_vector(2 downto 0);
signal W_I : std_logic_vector(9 downto 0); -- <10,0,t>
signal W_Q : std_logic_vector(9 downto 0); -- <10,0,t>

signal W_I_R : real :=0.0 ;
signal W_Q_R : real :=0.0 ;

begin

W1: WAVEGEN port map (CLK, RESET, OFFSET, W_I, W_Q);

-- System CLK generator
CLK <= not CLK after 5 ns;

-- TEST VECTOR
P1 : process
begin
OFFSET <= "001";
wait for 30 ns;
RESET <= '0';
wait for 700 ns;
OFFSET <= "010";
wait for 700 ns;
OFFSET <= "000";
wait for 700 ns;
OFFSET <= "011";
wait for 700 ns;
OFFSET <= "100";
wait for 700 ns;
```

```
OFFSET <= "101";
wait for 700 ns;
OFFSET <= "110";
wait for 700 ns;
OFFSET <= "111";
wait for 700 ns;
end process;


W_I_R <= real(CONV_INTEGER(signed(W_I))) /(2.0**9);
W_Q_R <= real(CONV_INTEGER(signed(W_Q))) /(2.0**9);

end;

configuration CFG_WAVEGEN of TESTBENCH_WAVEGEN is
for SIM_DATA
end for;
end;
```

・レポート

```
****************************************
Report : area
Design : WAVEGEN
Version: 2003.06
Date : Sat Dec 23 14:17:28 2006
****************************************

Library(s) Used:

class (File: /usr/local/synopsys/U-2003.06-dc/libraries/syn/class.db)

Number of ports: 25
Number of nets: 385
Number of cells: 362
Number of references: 16

Combinational area: 520.000000
Noncombinational area: 96.000000
Net Interconnect area: undefined (Wire load has zero net area)

Total cell area: 616.000000
Total area: undefined
1
design_analyzer> report_timing -path full -delay max -max_paths 1 -nworst 1

****************************************
Report : timing
-path full
-delay max
-max_paths 1
Design : WAVEGEN
Version: 2003.06
Date : Sat Dec 23 14:17:28 2006
****************************************

Operating Conditions:
Wire Load Model Mode: top

Startpoint: SUM_reg[0] (rising edge-triggered flip-flop clocked by CLK)
Endpoint: SUM_reg[5] (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: max
```

```
Des/Clust/Port Wire Load Model Library
-----------------------------------------------
WAVEGEN 05x05 class

Point Incr Path
-------------------------------------------------------------------------
clock CLK (rise edge) 0.00 0.00
clock network delay (ideal) 0.00 0.00
SUM_reg[0]/CP (FD1S) 0.00 0.00 r
SUM_reg[0]/Q (FD1S) 1.57 1.57 f
add_24/plus/B[0] (WAVEGEN_DW01_add_6_1) 0.00 1.57 f
add_24/plus/U5/Z (AN2I) 0.64 2.20 f
add_24/plus/U18/Z (ND2I) 0.25 2.45 r
add_24/plus/U20/Z (ND2I) 0.26 2.72 f
add_24/plus/U22/Z (ND2I) 0.25 2.97 r
add_24/plus/U24/Z (ND2I) 0.26 3.23 f
add_24/plus/U26/Z (ND2I) 0.25 3.49 r
add_24/plus/U28/Z (ND2I) 0.26 3.75 f
add_24/plus/U30/Z (ND2I) 0.25 4.00 r
add_24/plus/U32/Z (ND2I) 0.19 4.19 f
add_24/plus/U6/Z (ENI) 0.47 4.66 f
add_24/plus/SUM[5] (WAVEGEN_DW01_add_6_1) 0.00 4.66 f
SUM_reg[5]/TE (FD1S) 0.00 4.66 f
data arrival time 4.66

clock CLK (rise edge) 10.00 10.00
clock network delay (ideal) 0.00 10.00
SUM_reg[5]/CP (FD1S) 0.00 10.00 r
library setup time -1.30 8.70
data required time 8.70
-------------------------------------------------------------------------
data required time 8.70
data arrival time -4.66
-------------------------------------------------------------------------
slack (MET) 4.04
```



波形.png	Content-Type: image/png Content-Encoding: base64