CAD

-report3-

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1　問題 1

与えられた ALU 記述に対して以下をレポートせよ。

- scirocco での正常動作波形

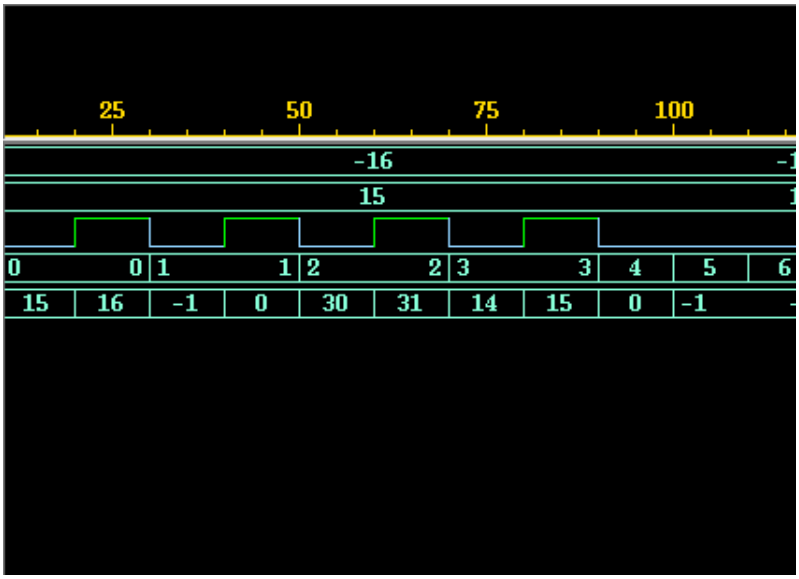

図 1: 正常動作波形

- 展開前の回路で、速度最小での回路図、面積、クリティカルパス遅延、クリテイカルパスの入力ピンと出力ピン。

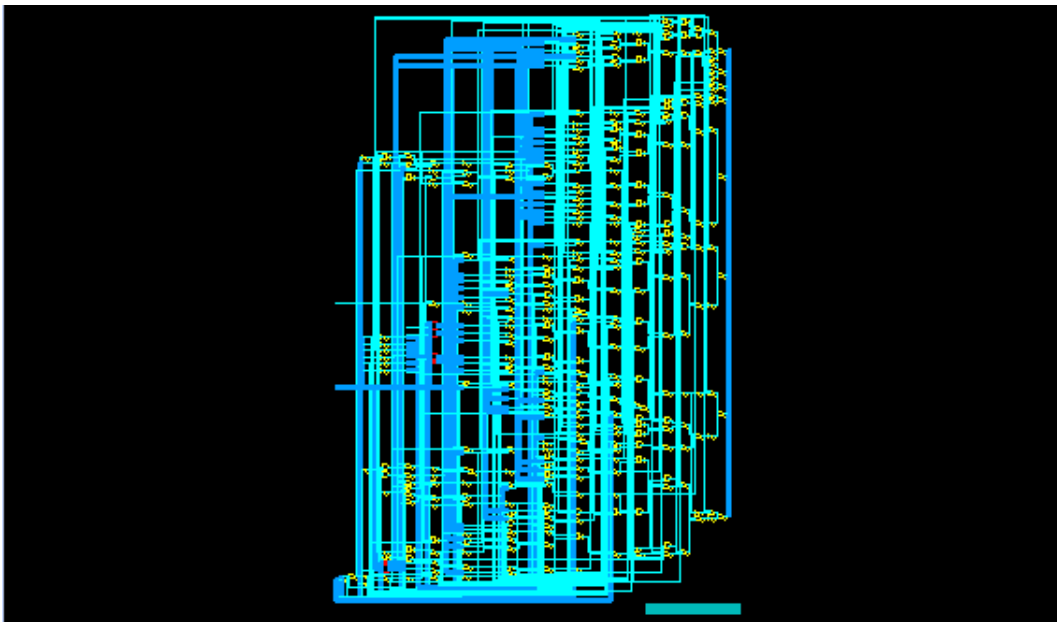

図 2: 展開前の回路図

```
****************************************
Report : area
Design : ALU
Version: 2003.06
Date   : Wed Nov 22 13:40:20 2006
****************************************

Library(s) Used:

    class (File: /usr/local/synopsys/U-2003.06-dc/libraries/syn/class.db)

Number of ports:               30
Number of nets:               394
Number of cells:              326
Number of references:          18

Combinational area:       1212.000000
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          1212.000000
Total area:                 undefined
1
design_analyzer> report_timing -path full -delay max -max_paths 1 -nworst 1

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
```

```
Design : ALU
Version: 2003.06
Date   : Wed Nov 22 13:40:20 2006
****************************************

Operating Conditions:
Wire Load Model Mode: top

  Startpoint: B[1] (input port)
  Endpoint: Y[5] (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ALU                10x10                 class

  Point                                                   Incr       Path
  ---------------------------------------------------------------------------
  input external delay                                    0.00       0.00 f
  B[1] (in)                                               0.00       0.00 f
  sub_41/minus/minus/B[1] (ALU_DW01_sub_8_0)              0.00       0.00 f
  sub_41/minus/minus/U37/Z (IVI)                          0.25       0.25 r
  sub_41/minus/minus/U30/Z (ND2I)                         0.13       0.38 f
  sub_41/minus/minus/U31/Z (IVI)                          0.25       0.63 r
  sub_41/minus/minus/U107/Z (ND2I)                        0.13       0.76 f
  sub_41/minus/minus/U35/Z (ND2I)                         0.31       1.06 r
  sub_41/minus/minus/U9/Z (IVI)                           0.13       1.19 f
  sub_41/minus/minus/U109/Z (ND2I)                        0.26       1.45 r
  sub_41/minus/minus/U110/Z (ND2I)                        0.13       1.58 f
  sub_41/minus/minus/U111/Z (ND2I)                        0.26       1.84 r
  sub_41/minus/minus/U91/Z (ENI)                          0.43       2.27 f
  sub_41/minus/minus/DIFF[5] (ALU_DW01_sub_8_0)           0.00       2.27 f
  U138/Z (ND2I)                                           0.26       2.53 r
  syn273/Z (AN2I)                                         0.35       2.87 r
  U131/Z (ND2I)                                           0.20       3.07 f
  U127/Z (AO7P)                                           0.70       3.77 r
  net7579/Z (ND2I)                                        0.22       3.99 f
  U124/Z (IVI)                                            0.31       4.29 r
  U123/Z (IVI)                                            0.13       4.42 f
  U122/Z (ND2I)                                           0.26       4.68 r
  U116/Z (ND2I)                                           0.06       4.74 f
  Y[5] (out)                                              0.00       4.74 f
  data arrival time                                                  4.74

  max_delay                                               0.00       0.00
  output external delay                                   0.00       0.00
  data required time                                                 0.00
  ---------------------------------------------------------------------------
  data required time                                                 0.00
  data arrival time                                                 -4.74
  ---------------------------------------------------------------------------
  slack (VIOLATED)                                                  -4.74


1
```

- 展開後の回路で、速度最小での回路図、面積、クリティカルパス遅延、クリテイカルパスの入力ピンと出力ピン。

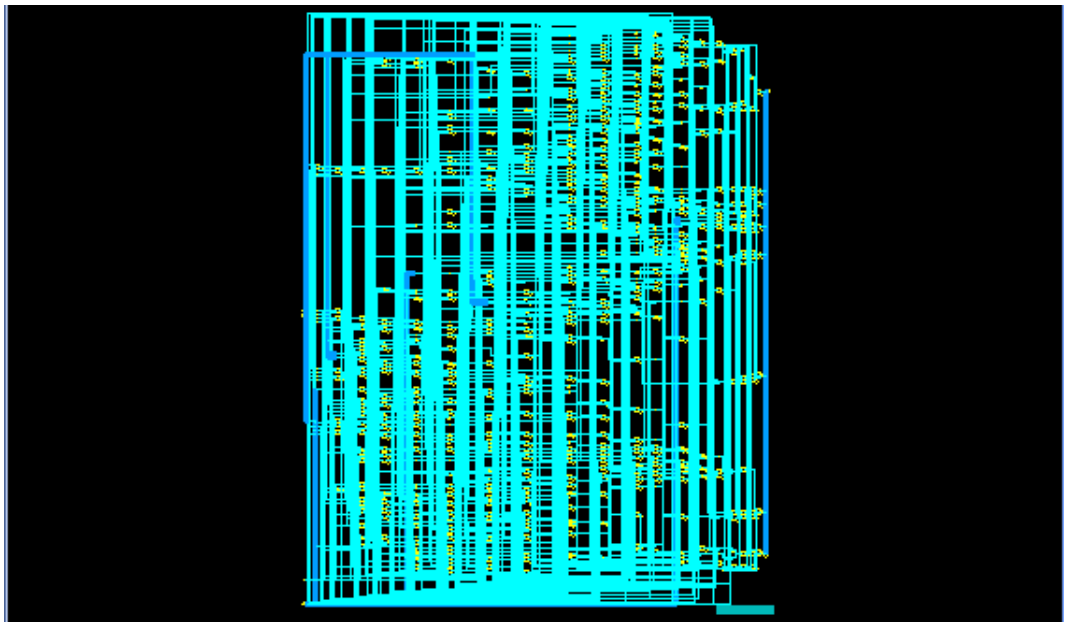

図 3: 展開後の回路図

```
****************************************
Report : area
Design : ALU
Version: 2003.06
Date   : Wed Nov 22 13:54:33 2006
****************************************

Library(s) Used:

    class (File: /usr/local/synopsys/U-2003.06-dc/libraries/syn/class.db)

Number of ports:               30
Number of nets:               784
Number of cells:              762
Number of references:          12

Combinational area:        968.000000
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           968.000000
Total area:                 undefined
1
design_analyzer> report_timing -path full -delay max -max_paths 1 -nworst 1

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
```

```
Design : ALU
Version: 2003.06
Date   : Wed Nov 22 13:54:33 2006
****************************************

Operating Conditions:
Wire Load Model Mode: top

  Startpoint: A[0] (input port)
  Endpoint: Y[5] (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ALU                05x05                 class

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  A[0] (in)                                0.00       0.00 f
  U1913/Z (B4IP)                           0.37       0.37 r
  U1911/Z (ND2I)                           0.12       0.49 f
  U1902/Z (ND2I)                           0.30       0.79 r
  U1905/Z (ND2I)                           0.12       0.91 f
  U1906/Z (ND2I)                           0.30       1.21 r
  U1988/Z (ND2I)                           0.20       1.41 f
  U1927/Z (ND2I)                           0.30       1.70 r
  U1914/Z (ND2I)                           0.12       1.83 f
  U1915/Z (ND2I)                           0.29       2.12 r
  U1983/Z (AO3P)                           0.55       2.67 f
  U1997/Z (AO7P)                           0.68       3.35 r
  U1998/Z (IVI)                            0.17       3.53 f
  U1864/Z (MUX21LP)                        0.58       4.11 r
  U1847/Z (ND2I)                           0.12       4.23 f
  U1848/Z (IVI)                            0.24       4.47 r
  U1877/Z (AO3)                            0.43       4.91 f
  Y[5] (out)                               0.00       4.91 f
  data arrival time                                   4.91

  max_delay                                0.00       0.00
  output external delay                    0.00       0.00
  data required time                                  0.00
  -----------------------------------------------------------
  data required time                                  0.00
  data arrival time                                  -4.91
  -----------------------------------------------------------
  slack (VIOLATED)                                   -4.91


1
```

- 展開による合成結果の差の考察。

  トータルエリアは, 展開前は 1212.000000 であったが, 展開後は 968.000000 となり。展開後の方が面積は小さくなった。しかしクリティカルパス遅延は, 展開前が 4.74 なのに対し, 展開後は 4.91 と増えている。この結果よりボックスを使わない方が面積は小さくなるがクリティカルパス遅延は増えることが分かる。

2　問題2

記述を変更して 4 ビットと１６ビットの同一機能の ALU を設計し、

- 制約なしで合成し,

  ４ビット、8 ビット、１６ビット ALU のビット幅と回路面積、およびビット幅と回路速度の関係を調べよ。

  以下は４ビット、8 ビット、１６ビット ALU の timing と area の report である。

  ４ビット

```
****************************************
Report : area
Design : ALU_4
Version: 2003.06
Date   : Wed Nov 22 21:01:18 2006
****************************************

Library(s) Used:

    class (File: /usr/local/synopsys/U-2003.06-dc/libraries/syn/class.db)

Number of ports:               18
Number of nets:               109
Number of cells:               95
Number of references:          16

Combinational area:        161.000000
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           161.000000
Total area:                 undefined
1
design_analyzer> report_timing -path full -delay max -max_paths 1 -nworst 1

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ALU_4
Version: 2003.06
Date   : Wed Nov 22 21:01:18 2006
****************************************

Operating Conditions:
Wire Load Model Mode: top

  Startpoint: CarryIn (input port)
  Endpoint: Y[1] (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
```

```
  ---------------------------------------------
  ALU_4              05x05                class

  Point                                   Incr       Path
  ------------------------------------------------------------
  input external delay                    0.00       0.00 r
  CarryIn (in)                            0.00       0.00 r
  U95/Z (IV)                              0.37       0.37 f
  U92/Z (ND2)                             1.34       1.72 r
  U144/Z (IV)                             0.37       2.09 f
  省略
  U172/Z (IV)                             0.30      11.72 f
  U167/Z (AO2)                            1.44      13.17 r
  U159/Z (EN)                             1.15      14.32 f
  U130/Z (AO2)                            1.18      15.50 r
  U148/Z (AO7)                            0.68      16.18 f
  U139/Z (AO2)                            1.18      17.36 r
  U85/Z (AO7)                             0.40      17.77 f
  Y[1] (out)                              0.00      17.77 f
  data arrival time                                 17.77
  ------------------------------------------------------------
  (Path is unconstrained)


1
```

8ビット

```
****************************************
Report : area
Design : ALU
Version: 2003.06
Date   : Wed Nov 22 21:13:20 2006
****************************************

Library(s) Used:

    class (File: /usr/local/synopsys/U-2003.06-dc/libraries/syn/class.db)

Number of ports:               30
Number of nets:               156
Number of cells:              127
Number of references:           9

Combinational area:        298.000000
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           298.000000
Total area:                 undefined
1
design_analyzer> report_timing -path full -delay max -max_paths 1 -nworst 1

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ALU
Version: 2003.06
Date   : Wed Nov 22 21:13:20 2006
****************************************

Operating Conditions:
Wire Load Model Mode: top

  Startpoint: CarryIn (input port)
  Endpoint: Y[5] (output port)
  Path Group: (none)
  Path Type: max
```

```
  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ALU                05x05                 class

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  CarryIn (in)                             0.00       0.00 f
  U100/Z (IV)                              1.27       1.27 r
  U109/Z (AO2)                             0.58       1.85 f
  U121/Z (NR2)                             3.06       4.91 r
  U188/Z (AO2)                             0.58       5.49 f
  U83/Z (OR3)                              1.42       6.92 f
  r32/B[0] (ALU_DW01_addsub_8_0)           0.00       6.92 f
  r32/U41/Z (EO1)                          1.35       8.27 f
  省略
  r32/U39/Z (IV)                           0.43      19.72 f
  r32/U42/Z (EO1)                          1.44      21.17 r
  r32/U14/Z (EO)                           1.15      22.32 f
  r32/SUM[6] (ALU_DW01_addsub_8_0)         0.00      22.32 f
  U129/Z (AO2)                             1.18      23.50 r
  U150/Z (ND2)                             0.45      23.95 f
  U134/Z (AO2)                             1.18      25.13 r
  U87/Z (AO7)                              0.40      25.54 f
  Y[5] (out)                               0.00      25.54 f
  data arrival time                                  25.54
  -----------------------------------------------------------
  (Path is unconstrained)


1
```

１６ビット

```
****************************************
Report : area
Design : ALU_16
Version: 2003.06
Date   : Wed Nov 22 21:06:59 2006
****************************************

Library(s) Used:

    class (File: /usr/local/synopsys/U-2003.06-dc/libraries/syn/class.db)

Number of ports:               54
Number of nets:               275
Number of cells:              222
Number of references:          12

Combinational area:        557.000000
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           557.000000
Total area:                 undefined
1
design_analyzer> report_timing -path full -delay max -max_paths 1 -nworst 1

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ALU_16
Version: 2003.06
Date   : Wed Nov 22 21:06:59 2006
****************************************

Operating Conditions:
```

```
Wire Load Model Mode: top

  Startpoint: CarryIn (input port)
  Endpoint: Y[14] (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ALU_16             05x05                 class

  Point                                                    Incr       Path
  ---------------------------------------------------------------------------
  input external delay                                     0.00       0.00 f
  CarryIn (in)                                             0.00       0.00 f
  U126/Z (IV)                                              1.44       1.44 r
  U149/Z (AO2)                                             0.58       2.02 f
  U185/Z (NR2)                                             5.52       7.54 r
  U283/Z (AO2)                                             0.58       8.12 f
  U83/Z (OR3)                                              1.42       9.55 f
  r32/B[0] (ALU_16_DW01_addsub_16_0)                       0.00       9.55 f
  r32/U78/Z (EO1)                                          1.35      10.90 f
  r32/U33/Z (AO5)                                          2.10      13.00 r
  r32/U4/Z (ND2)                                           0.25      13.25 f
  r32/U35/Z (EO1)                                          2.06      15.32 r
  r32/U36/Z (AO5)                                          0.75      16.06 f
  r32/U5/Z (OR2)                                           0.93      16.99 f
  r32/U38/Z (AO2)                                          2.06      19.06 r
  r32/U39/Z (AO5)                                          0.75      19.80 f
  r32/U6/Z (OR2)                                           0.93      20.74 f
  r32/U41/Z (AO2)                                          2.06      22.80 r
  省略
  r32/U62/Z (EO)                                           1.15      38.71 f
  r32/SUM[15] (ALU_16_DW01_addsub_16_0)                    0.00      38.71 f
  U255/Z (ND2)                                             0.69      39.40 r
  U256/Z (AO3)                                             0.68      40.08 f
  U210/Z (AO2)                                             1.18      41.26 r
  U86/Z (AO7)                                              0.40      41.66 f
  Y[14] (out)                                              0.00      41.66 f
  data arrival time                                                  41.66
  ---------------------------------------------------------------------------
  (Path is unconstrained)


1
```

面積はビット幅が二倍になると約 1.7 倍になり, 回路速度はビット幅が二倍になると約 1.5 倍になっている。以上の結果よりビット幅と比例の関係にあると言える。

- 最小速度で合成し,

  ４ビット、8 ビット、１６ビット ALU のビット幅と回路面積、およびビット幅と回路速度の関係を調べよ。

  以下は４ビット、8 ビット、１６ビット ALU の timing と area の report である。

４ビット

```
****************************************
Report : area
Design : ALU_4
Version: 2003.06
Date   : Wed Nov 22 21:04:29 2006
****************************************

Library(s) Used:

    class (File: /usr/local/synopsys/U-2003.06-dc/libraries/syn/class.db)

Number of ports:               18
Number of nets:               183
Number of cells:              169
Number of references:          10

Combinational area:        235.000000
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           235.000000
Total area:                 undefined
1
design_analyzer> report_timing -path full -delay max -max_paths 1 -nworst 1

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ALU_4
Version: 2003.06
Date   : Wed Nov 22 21:04:29 2006
****************************************

Operating Conditions:
Wire Load Model Mode: top

  Startpoint: Sel[0] (input port)
  Endpoint: Y[1] (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ALU_4              05x05                 class

  Point                                    Incr       Path
  ----------------------------------------------------------
  input external delay                     0.00       0.00 r
  Sel[0] (in)                              0.00       0.00 r
  U216/Z (IVI)                             0.12       0.12 f
  U214/Z (ND2I)                            0.25       0.38 r
  省略
  U221/Z (IVI)                             0.12       2.31 f
  syn643/Z (ND2I)                          0.30       2.61 r
  U220/Z (ENI)                             0.42       3.03 f
  U248/Z (ND2I)                            0.25       3.28 r
  U193/Z (ND2I)                            0.19       3.47 f
  U192/Z (MUX21LP)                         0.58       4.05 r
  net4304/Z (ND2I)                         0.12       4.18 f
  U182/Z (ND2I)                            0.21       4.39 r
  Y[1] (out)                               0.00       4.39 r
  data arrival time                                   4.39

  max_delay                                0.00       0.00
  output external delay                    0.00       0.00
  data required time                                  0.00
```

```
  ------------------------------------------------------------
  data required time                                    0.00
  data arrival time                                    -4.39
  ------------------------------------------------------------
  slack (VIOLATED)                                     -4.39


1
```

8ビット

```
****************************************
Report : area
Design : ALU
Version: 2003.06
Date   : Wed Nov 22 21:15:49 2006
****************************************

Library(s) Used:

    class (File: /usr/local/synopsys/U-2003.06-dc/libraries/syn/class.db)

Number of ports:               30
Number of nets:               212
Number of cells:              182
Number of references:          13

Combinational area:        530.000000
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           530.000000
Total area:                 undefined
1
design_analyzer> report_timing -path full -delay max -max_paths 1 -nworst 1

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ALU
Version: 2003.06
Date   : Wed Nov 22 21:15:49 2006
****************************************

Operating Conditions:
Wire Load Model Mode: top

  Startpoint: Sel[1] (input port)
  Endpoint: Y[6] (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ALU                05x05                 class

  Point                                    Incr       Path
  ------------------------------------------------------------
  input external delay                     0.00       0.00 f
  Sel[1] (in)                              0.00       0.00 f
  U226/Z (IVI)                             0.24       0.24 r
  U225/Z (ND2I)                            0.19       0.43 f
  U222/Z (MUX21LP)                         0.65       1.08 r
  U217/Z (MUX21LP)                         0.41       1.48 f
  U218/Z (IVI)                             0.24       1.73 r
  net3669/Z (ND2I)                         0.20       1.92 f
```

```
  r32/B[0] (ALU_DW01_addsub_8_0)          0.00       1.92 f
  r32/U61/Z (ENI)                         0.46       2.39 r
  省略
  U252/Z (NR2I)                           0.57       5.96 r
  U244/Z (ND2I)                           0.12       6.08 f
  U245/Z (ND2I)                           0.25       6.33 r
  U263/Z (IVI)                            0.07       6.40 f
  Y[6] (out)                              0.00       6.40 f
  data arrival time                                  6.40

  max_delay                               0.00       0.00
  output external delay                   0.00       0.00
  data required time                                 0.00
  ------------------------------------------------------------
  data required time                                 0.00
  data arrival time                                 -6.40
  ------------------------------------------------------------
  slack (VIOLATED)                                  -6.40


1
```

１６ビット

```
****************************************
Report : area
Design : ALU_16
Version: 2003.06
Date   : Wed Nov 22 21:11:12 2006
****************************************

Library(s) Used:

    class (File: /usr/local/synopsys/U-2003.06-dc/libraries/syn/class.db)

Number of ports:              54
Number of nets:              407
Number of cells:             351
Number of references:         16

Combinational area:       1013.000000
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          1013.000000
Total area:                 undefined
1
design_analyzer> report_timing -path full -delay max -max_paths 1 -nworst 1

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : ALU_16
Version: 2003.06
Date   : Wed Nov 22 21:11:12 2006
****************************************

Operating Conditions:
Wire Load Model Mode: top

  Startpoint: Sel[0] (input port)
  Endpoint: Y[13] (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
```

```
  ---------------------------------------------
  ALU_16             10x10                class

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
  input external delay                                    0.00       0.00 f
  Sel[0] (in)                                             0.00       0.00 f
  U342/Z (IVI)                                            0.25       0.25 r
  U341/Z (ND2I)                                           0.20       0.44 f
  省略
  r32/U25/Z (IVI)                                         0.13       3.44 f
  r32/U23/Z (NR2I)                                        0.59       4.04 r
  r32/U9/Z (ND2I)                                         0.13       4.17 f
  r32/U10/Z (IVI)                                         0.31       4.47 r
  r32/U29/Z (ND2I)                                        0.13       4.60 f
  r32/U30/Z (ND2I)                                        0.30       4.90 r
  r32/U33/Z (MUX21L)                                      0.95       5.84 r
  r32/SUM[12] (ALU_16_DW01_addsub_16_1)                   0.00       5.84 r
  U327/Z (ND2I)                                           0.13       5.97 f
  net7794/Z (ND2I)                                        0.31       6.28 r
  net6056/Z (ND2I)                                        0.20       6.48 f
  U318/Z (AO3P)                                           0.57       7.05 r
  Y[13] (out)                                             0.00       7.05 r
  data arrival time                                                  7.05

  max_delay                                               0.00       0.00
  output external delay                                   0.00       0.00
  data required time                                                 0.00
  ------------------------------------------------------------------------
  data required time                                                 0.00
  data arrival time                                                 -7.05
  ------------------------------------------------------------------------
  slack (VIOLATED)                                                  -7.05


1
```

面積はビット幅が二倍になると約 2 倍になったが, 回路速度はビット幅が４ビットから８ビットになると約 1.5 倍になり, ８ビットから１６ビットになると約 1.1 倍になり制約なしの場合よりばらつきが増えている。