CAD

-report4-

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1　宿題 4-1

1.1　問題 1

クロックの周期のターゲット値を 1 として、再合成する。（なるべく、最小サイクル時間の小さい回路を合成せよ）

クロックの周期のターゲット値を 1 として合成し,BOX を ungroup したときの report の抜粋を以下に示す。

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : AVG4
Version: 2003.06
Date   : Wed Dec  6 17:23:50 2006
****************************************

Operating Conditions:
Wire Load Model Mode: top

  Startpoint: FF1_reg[1] (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: AVGOUT_reg[7]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  AVG4               05x05                 class

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLK (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  FF1_reg[1]/CP (FD1)                      0.00       0.00 r
  FF1_reg[1]/Q (FD1)                       1.57       1.57 f
  add_29/plus/U18/Z (NR2I)                 0.57       2.14 r
  add_29/plus/U53/Z (NR2I)                 0.20       2.34 f
  add_29/plus/U84/Z (ND2I)                 0.30       2.64 r
  add_29/plus/U65/Z (ND2I)                 0.12       2.76 f
  add_29/plus/U17/Z (NR2I)                 0.73       3.49 r
  add_29/plus/U8/Z (MUX21LP)               0.98       4.47 r
省略
  AVGOUT_reg[7]/D (FD1)                    0.00       9.84 f
  data arrival time                                   9.84

  clock CLK (rise edge)                    1.00       1.00
  clock network delay (ideal)              0.00       1.00
  AVGOUT_reg[7]/CP (FD1)                   0.00       1.00 r
  library setup time                      -0.80       0.20
  data required time                                  0.20
  -----------------------------------------------------------
  data required time                                  0.20
  data arrival time                                  -9.84
  -----------------------------------------------------------
  slack (VIOLATED)                                   -9.64
```

1

1.2　問題 2

この時の最小の動作サイクル時間はいくらか？

clock CLK (rise edge) が 1.00ns で,slack (VIOLATED) が-9.64 であるから最小動作サイクル時間は
$1.00 - (-9.64) = 10.64$
となる。

2　宿題 4-2

回路を改造して、１６ポイントの平均を計算する回路を設計せよ。
以下のものを提出すること。

- scirocco の正常動作波形
- 設計した回路とテストベンチの VHDL 記述
- なるべくサイクル時間が小さくなるように合成した回路の、回路図、面積レポート、最小サイクル時間

2.1　正常動作波形

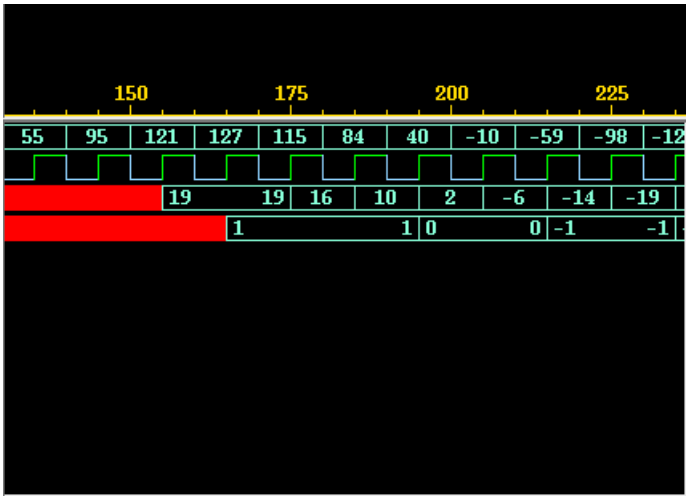

図 1: 波形

FF1 から FF16 までの全てに数値が入っていないと合計, 平均がだせないので, SUM は 155ns,AVGOUT は 165ns まで数値が入っていない。

2.2 設計した回路とテストベンチの VHDL 記述

avg16.vhd

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_ARITH.all;

entity AVG16 is
  port(CLK     : in  std_logic;
       FMINPUT : in  std_logic_vector(7 downto 0);
       AVGOUT  : out std_logic_vector(7 downto 0));
end AVG16;

architecture RTL of AVG16 is

signal FF1, FF2, FF3, FF4 : std_logic_vector(7 downto 0);
signal FF5, FF6, FF7, FF8 : std_logic_vector(7 downto 0);
signal FF9, FF10, FF11, FF12 : std_logic_vector(7 downto 0);
signal FF13, FF14, FF15, FF16 : std_logic_vector(7 downto 0);
signal SUM    : std_logic_vector(11 downto 0);

begin

-- SHIFT REGISTER
  process(CLK) begin
    if (CLK'event and CLK = '1') then
       FF1 <= FMINPUT;
       FF2 <= FF1;
       FF3 <= FF2;
       FF4 <= FF3;
       FF5 <= FF4;
       FF6 <= FF5;
       FF7 <= FF6;
       FF8 <= FF7;
       FF9 <= FF8;
       FF10 <= FF9;
       FF11 <= FF10;
       FF12 <= FF11;
       FF13 <= FF12;
       FF14 <= FF13;
       FF15 <= FF14;
       FF16 <= FF15;
    end if;
  end process;

-- SUM
  SUM <= signed(FF1(7)&FF1(7)&FF1(7)&FF1(7)&FF1)
         +signed(FF2(7)&FF2(7)&FF2(7)&FF2(7)&FF2)
         +signed(FF3(7)&FF3(7)&FF3(7)&FF3(7)&FF3)
         +signed(FF4(7)&FF4(7)&FF4(7)&FF4(7)&FF4)
         +signed(FF5(7)&FF5(7)&FF5(7)&FF5(7)&FF5)
         +signed(FF6(7)&FF6(7)&FF6(7)&FF6(7)&FF6)
         +signed(FF7(7)&FF7(7)&FF7(7)&FF7(7)&FF7)
         +signed(FF8(7)&FF8(7)&FF8(7)&FF8(7)&FF8)
         +signed(FF9(7)&FF9(7)&FF9(7)&FF9(7)&FF9)
         +signed(FF10(7)&FF10(7)&FF10(7)&FF10(7)&FF10)
         +signed(FF11(7)&FF11(7)&FF11(7)&FF11(7)&FF11)
         +signed(FF12(7)&FF12(7)&FF12(7)&FF12(7)&FF12)
         +signed(FF13(7)&FF13(7)&FF13(7)&FF13(7)&FF13)
         +signed(FF14(7)&FF14(7)&FF14(7)&FF14(7)&FF14)
         +signed(FF15(7)&FF15(7)&FF15(7)&FF15(7)&FF15)
         +signed(FF16(7)&FF16(7)&FF16(7)&FF16(7)&FF16);

-- DIVIDE BY 16 (SHIFT 4 bit), OUTPUT REGISTER
  process(CLK) begin
```

```
    if (CLK'event and CLK='1') then
        AVGOUT <= SUM(11 downto 4);
    end if;
  end process;

end RTL;
```

SigGen16.vhd(テストベンチ)

```
library STD, IEEE;
use STD.TEXTIO.all;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_textio.all;

entity TESTBENCH_FF16 is
end TESTBENCH_FF16;

architecture SIM_DATA of TESTBENCH_FF16 is

component AVG16
  port(CLK     : in  std_logic;
       FMINPUT : in  std_logic_vector(7 downto 0);
       AVGOUT  : out std_logic_vector(7 downto 0));
end component;

signal FMINPUT    : std_logic_vector(7 downto 0);
signal AVGOUT     : std_logic_vector(7 downto 0);
signal CLK        : std_logic := '0';

begin

-- Sysetem CLK generation
      CLK <= not CLK after 5 ns;

-- DUT
  U1: AVG16 port map (CLK, FMINPUT, AVGOUT);

-- TEST VECTOR
  P1: process
      file TEST_IN  : text is in "fm.txt";
      variable LINE_IN : line;
      variable V_FMINPUT : std_logic_vector(7 downto 0);
  begin
      readline(TEST_IN, LINE_IN);
      read(LINE_IN, V_FMINPUT);
      FMINPUT <= V_FMINPUT;
      wait for 10 ns;
      if endfile(TEST_IN) then
        wait;
      end if;
  end process;

end SIM_DATA;

configuration CFG_FF16 of TESTBENCH_FF16 is
  for SIM_DATA
  end for;
end CFG_FF16;
```

2.3　回路図, 面積レポート, 最小サイクル時間

回路図を以下に示す。

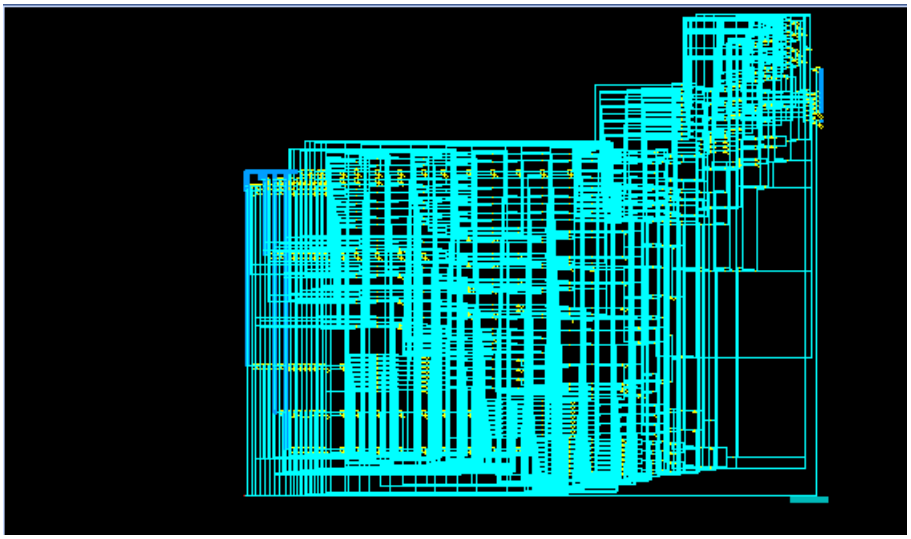

図 2: 回路図

area と timing の report を以下に示す。

```
****************************************
Report : area
Design : AVG16
Version: 2003.06
Date   : Wed Dec  6 20:58:40 2006
****************************************

Library(s) Used:

    class (File: /usr/local/synopsys/U-2003.06-dc/libraries/syn/class.db)

Number of ports:               17
Number of nets:              1282
Number of cells:             1273
Number of references:           7

Combinational area:       1576.000000
Noncombinational area:     952.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          2528.000000
Total area:                 undefined
1
design_analyzer> report_timing -path full -delay max -max_paths 1 -nworst 1
Information: Updating design information... (UID-85)

****************************************
Report : timing
        -path full
        -delay max
```

```
       -max_paths 1
Design : AVG16
Version: 2003.06
Date   : Wed Dec  6 20:58:40 2006
****************************************

Operating Conditions:
Wire Load Model Mode: top

  Startpoint: FF3_reg[0] (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: AVGOUT_reg[7]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  AVG16              20x20                 class

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLK (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  FF3_reg[0]/CP (FD1)                      0.00       0.00 r
  FF3_reg[0]/Q (FD1)                       1.63       1.63 f
  add_51/plus/U16/Z (ND2I)                 0.33       1.96 r
  add_51/plus/U37/Z (IVI)                  0.23       2.19 f
  add_51/plus/U44/Z (ND2I)                 0.27       2.46 r
  add_51/plus/U45/Z (ND2I)                 0.32       2.77 f
  add_51/plus/U47/Z (ND2I)                 0.27       3.04 r
  add_51/plus/U48/Z (ND2I)                 0.32       3.36 f
  add_51/plus/U50/Z (ND2I)                 0.27       3.63 r
  add_51/plus/U52/Z (ND2I)                 0.32       3.95 f
  add_51/plus/U55/Z (ND2I)                 0.27       4.22 r
  add_51/plus/U56/Z (ND2I)                 0.32       4.54 f
  add_51/plus/U58/Z (ND2I)                 0.27       4.81 r
  add_51/plus/U59/Z (ND2I)                 0.32       5.13 f
  add_51/plus/U61/Z (ND2I)                 0.27       5.40 r
  add_51/plus/U62/Z (ND2I)                 0.32       5.72 f
  add_51/plus/U5/Z (AN2I)                  0.84       6.55 f
  add_51/plus/U34/Z (MUX21L)               1.15       7.70 r
  add_54/plus/U89/Z (ENI)                  0.44       8.14 f
  add_54/plus/U7/Z (ENI)                   0.63       8.77 f
  add_58/plus/U89/Z (ENI)                  0.44       9.22 f
  add_58/plus/U7/Z (ENI)                   0.63       9.85 f
  add_59/plus/U26/Z (IVI)                  0.26      10.11 r
  add_59/plus/U58/Z (ND2I)                 0.15      10.26 f
  add_59/plus/U59/Z (ND2I)                 0.27      10.53 r
  add_59/plus/U61/Z (ND2I)                 0.32      10.85 f
  add_59/plus/U67/Z (ND2I)                 0.27      11.12 r
  add_59/plus/U69/Z (ND2I)                 0.32      11.44 f
  add_59/plus/U71/Z (ND2I)                 0.27      11.71 r
  add_59/plus/U73/Z (ND2I)                 0.22      11.93 f
  add_59/plus/U12/Z (ENI)                  0.44      12.37 f
  AVGOUT_reg[7]/D (FD1)                    0.00      12.37 f
  data arrival time                                  12.37

  clock CLK (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  AVGOUT_reg[7]/CP (FD1)                   0.00      10.00 r
  library setup time                      -0.80       9.20
  data required time                                  9.20
  -----------------------------------------------------------
  data required time                                  9.20
  data arrival time                                 -12.37
  -----------------------------------------------------------
  slack (VIOLATED)                                   -3.17


1
```

clock CLK (rise edge) が 10.00 で、slack (VIOLATED) が -3.17 であるから
最小動作サイクル時間は 13.17 となる。