

CAD  
-report6-

055702B

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## 1 動作波形

動作波形を以下に示す。

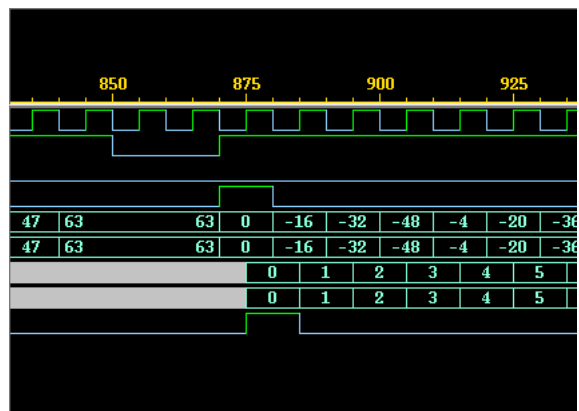


図 1: 動作波形

## 2 回路図

回路図を以下に示す。

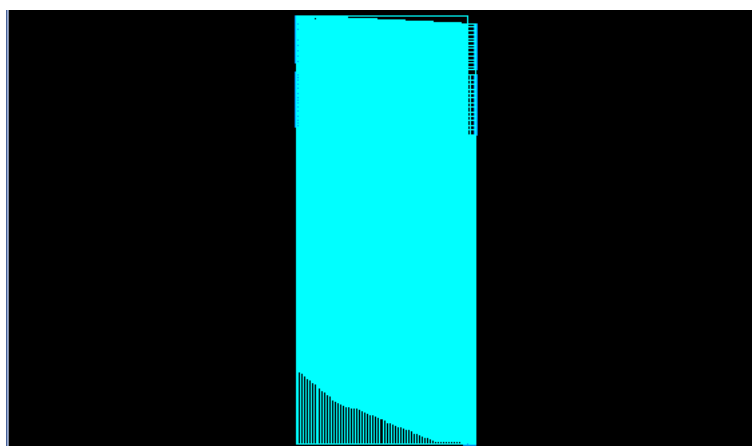


図 2: 回路図

### 3 report

```
*****
Report : area
Design : REORDER
Version: 2003.06
Date   : Fri Dec 29 16:31:21 2006
*****
```

Library(s) Used:

```
class (File: /usr/local/synopsys/U-2003.06-dc/libraries/syn/class.db)
```

```
Number of ports:      60
Number of nets:      18020
Number of cells:     17901
Number of references: 15
```

```
Combinational area: 18056.000000
Noncombinational area: 25365.000000
Net Interconnect area: undefined (Wire load has zero net area)
```

```
Total cell area: 43421.000000
Total area: undefined
```

```
1
design_analyzer> report_timing -path full -delay max -max_paths 1 -nworst 1
```

```
*****
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : REORDER
Version: 2003.06
Date   : Fri Dec 29 16:31:22 2006
*****
```

# A fanout number of 1000 was used for high fanout net computations.

Operating Conditions:  
Wire Load Model Mode: top

```
Startpoint: BANKEN_reg (rising edge-triggered flip-flop clocked by CLK)
Endpoint:   REGO_I_reg[4][8]
            (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type:  max
```

Des/Clust/Port	Wire Load Model	Library
REORDER	20x20	class

Point	Incr	Path
clock CLK (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
BANKEN_reg/CP (FD2)	0.00 #	0.00 r
BANKEN_reg/QN (FD2)	2.17	2.17 f
U137/Z (B4I)	20.00	22.17 r
U136/Z1 (B2I)	0.88	23.05 f
U14329/Z (IVI)	6.50	29.55 r
U14258/Z (ND2I)	9.55	39.10 f
U124/Y (IVDAP)	0.70	39.79 r
U14338/Z (IVI)	8.00	47.79 f
U12371/Z (NR2I)	0.65	48.44 r
U3137/Z (OR3)	0.75	49.18 r
REGO_I_reg[4][8]/D (FD1)	0.00	49.18 r
data arrival time		49.18
clock CLK (rise edge)	50.00	50.00
clock network delay (ideal)	0.00	50.00
REGO_I_reg[4][8]/CP (FD1)	0.00	50.00 r
library setup time	-0.80	49.20

data required time	49.20
-----	
data required time	49.20
data arrival time	-49.18
-----	
slack (MET)	0.02

1  
design\_analyzer>  
Thank you...