CAD

-report7-

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1 正常動作波形

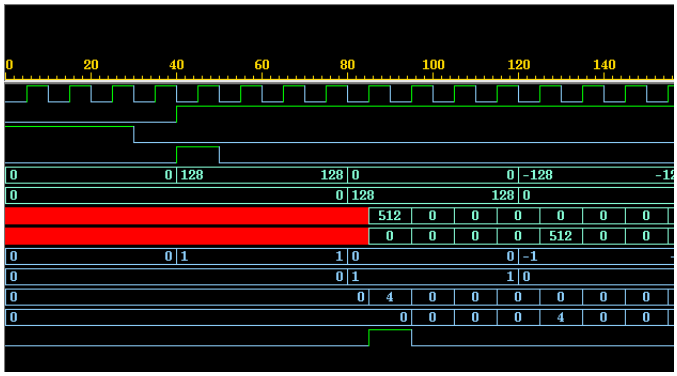

図 1: 正常動作波形

2 回路図

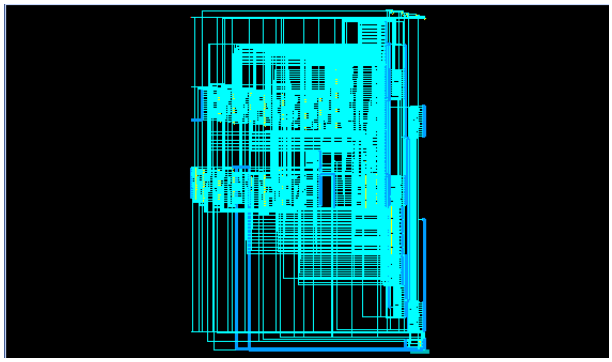

図 2: 回路図

3 Report

```
****************************************
Report : area
Design : STAGE3
Version: 2003.06
Date   : Thu Jan 25 18:16:00 2007
****************************************

Library(s) Used:

    class (File: /usr/local/synopsys/U-2003.06-dc/libraries/syn/class.db)
```

```
Number of ports:               61
Number of nets:              1558
Number of cells:             1210
Number of references:          18

Combinational area:       3084.000000
Noncombinational area:    1667.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          4751.000000
Total area:                 undefined
1
design_analyzer> report_timing -path full -delay max -max_paths 1 -nworst 1

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : STAGE3
Version: 2003.06
Date   : Thu Jan 25 18:16:00 2007
****************************************

Operating Conditions:
Wire Load Model Mode: top

  Startpoint: COUNT_reg[1]
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: COUNT_reg[5]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  STAGE3             20x20                 class

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock CLK (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  COUNT_reg[1]/CP (FD2)                                   0.00       0.00 r
  COUNT_reg[1]/Q (FD2)                                   16.29      16.29 r
  add_70/plus/A[1] (STAGE3_DW01_inc_6_0)                  0.00      16.29 r
  add_70/plus/U6/Z (AN3)                                  1.19      17.48 r
  add_70/plus/U9/Z (ND2I)                                 0.32      17.80 f
  add_70/plus/U14/Z (IVI)                                 0.26      18.06 r
  add_70/plus/U15/Z (ND2I)                                0.22      18.27 f
  add_70/plus/U10/Z (ENI)                                 0.44      18.72 f
  add_70/plus/SUM[5] (STAGE3_DW01_inc_6_0)                0.00      18.72 f
  U388/Z (ND2I)                                           0.27      18.99 r
  U207/Z (ND2I)                                           0.15      19.14 f
  COUNT_reg[5]/D (FD2)                                    0.00      19.14 f
  data arrival time                                                 19.14

  clock CLK (rise edge)                                  50.00      50.00
  clock network delay (ideal)                             0.00      50.00
  COUNT_reg[5]/CP (FD2)                                   0.00      50.00 r
  library setup time                                     -0.85      49.15
  data required time                                                49.15
  --------------------------------------------------------------------------
  data required time                                                49.15
  data arrival time                                                -19.14
  --------------------------------------------------------------------------
  slack (MET)                                                       30.01
```

4　テストベンチで計算されている、4FFT の入力値と出力値の関係

入力４点ごとに出力を計算する。ただし、同じ入力値を４回使用して、出力を４つ計算する。計算方法はフェーズごとに若干違う (符号が違う)。正常動作波形での最初の４つ出力値の計算方法を以下に示す。

1. フェーズ 1
   $S3OUT\_I = 128 + 128 + 128 + 128 = 512$
   $S3OUT\_Q = 0 + 0 + 0 + 0 = 0$
2. フェーズ 2
   $S3OUT\_I = 128 - 128 - 128 + 128 = 0$
   $S3OUT\_Q = 0 - 0 - 0 + 0 = 0$
3. フェーズ 3
   $S3OUT\_I = 128 - 128 + 128 - 128 = 0$
   $S3OUT\_Q = 0 - 0 + 0 - 0 = 0$
4. フェーズ 4
   $S3OUT\_I = 128 + 128 - 128 - 128 = 0$
   $S3OUT\_Q = 0 + 0 + 0 + 0 = 0$