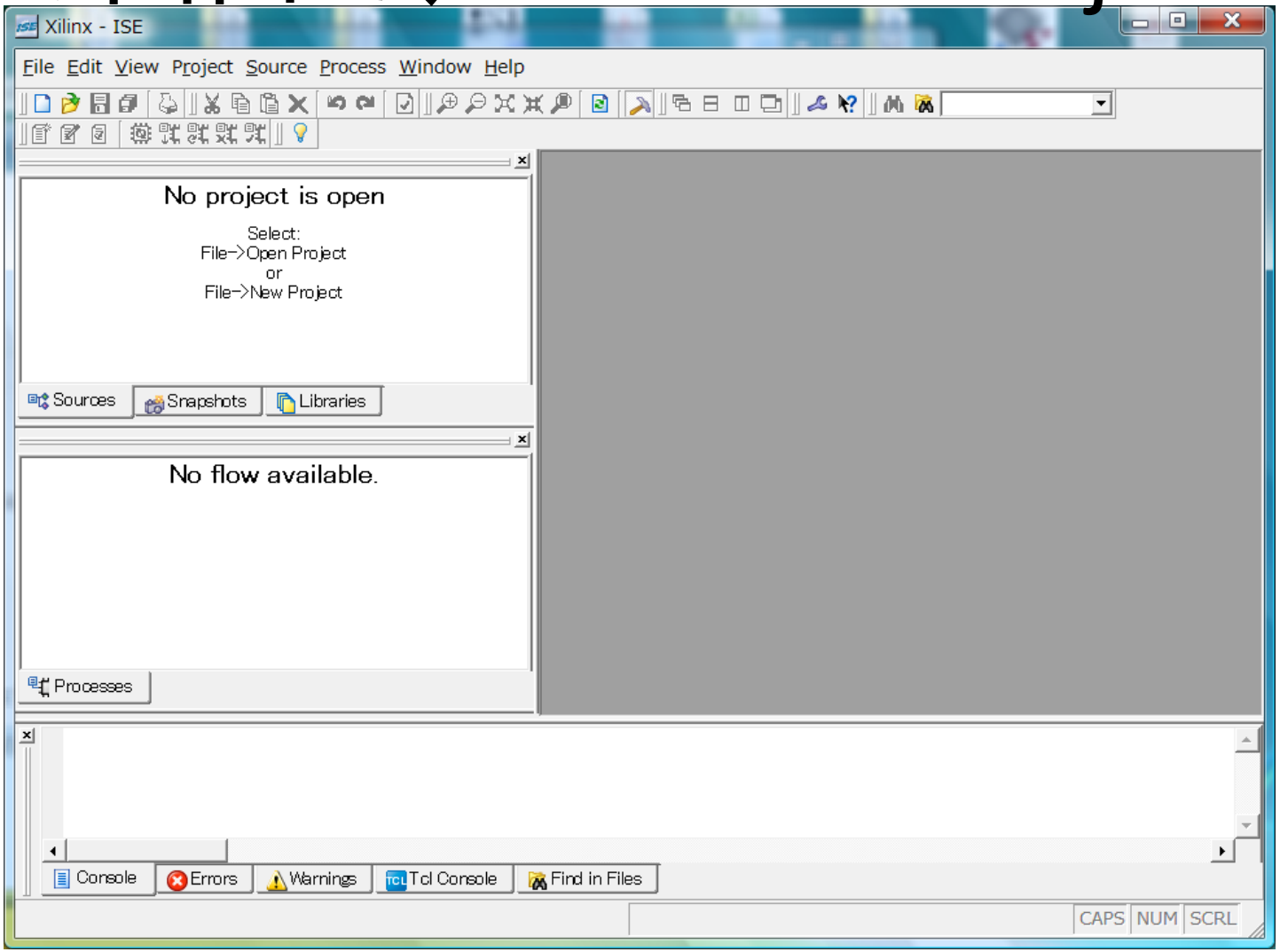
（1） ISEを使用して、
VHDLシミュレーションをする。

必要ファイルを以下よりダウンロード

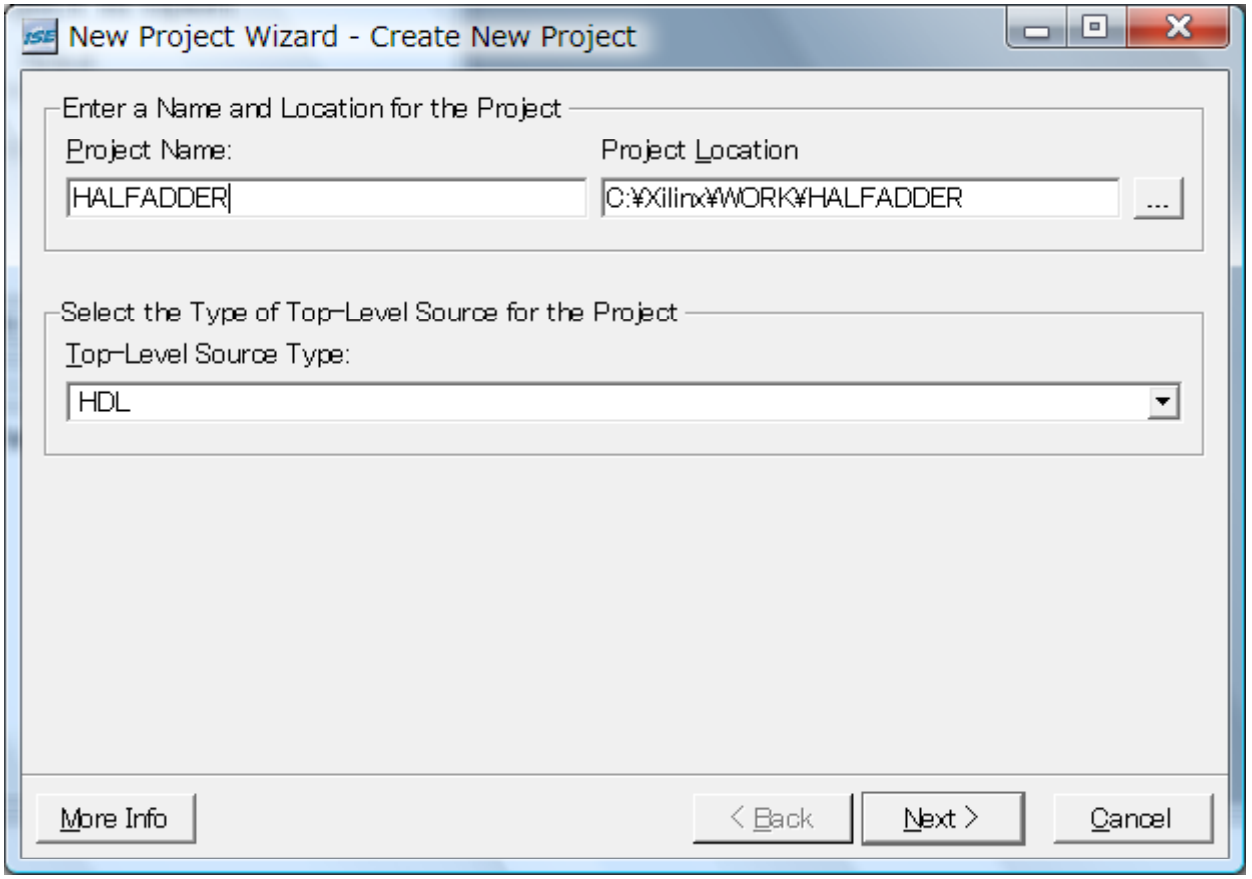
吉田先生の教科書サポートページ

- http://www.fts.ie.u-ryukyu.ac.jp/support/vhdl_digital/VHDL-src.html
- 3. HALF_ADDER-std.vhd
- 14. TESTBENCH_HA.vhd

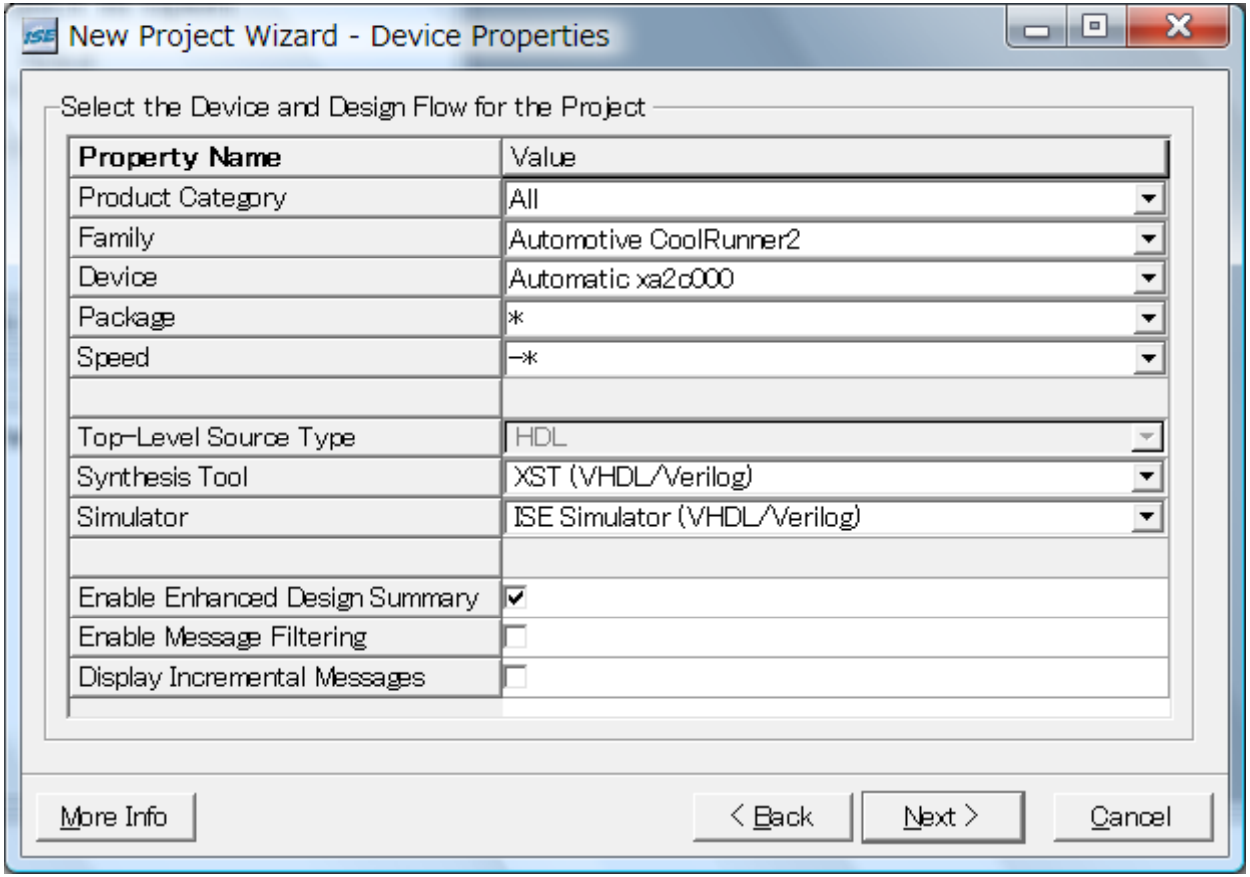
ISEを起動して
この画面で、File-> New Project



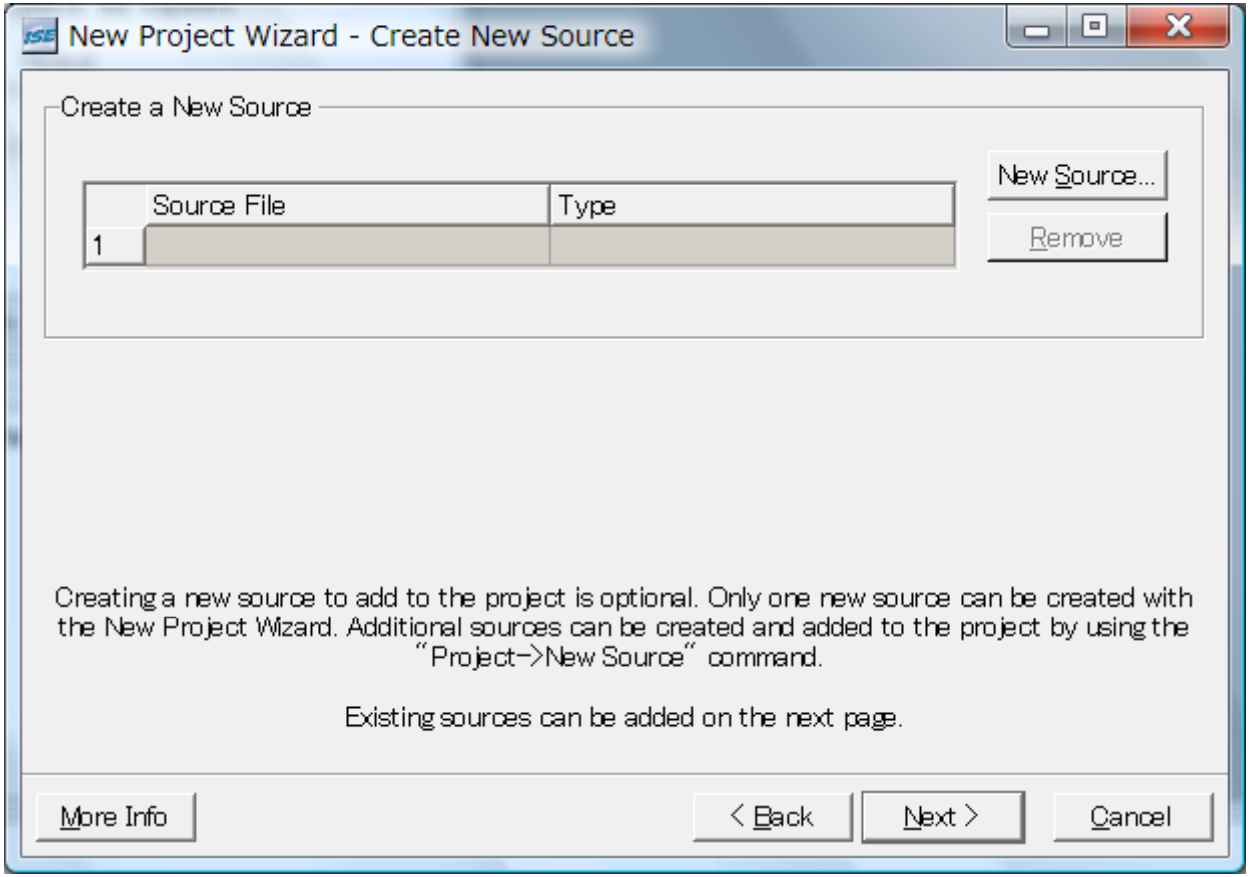
お好みのディレクトリと
プロジェクト名を設定



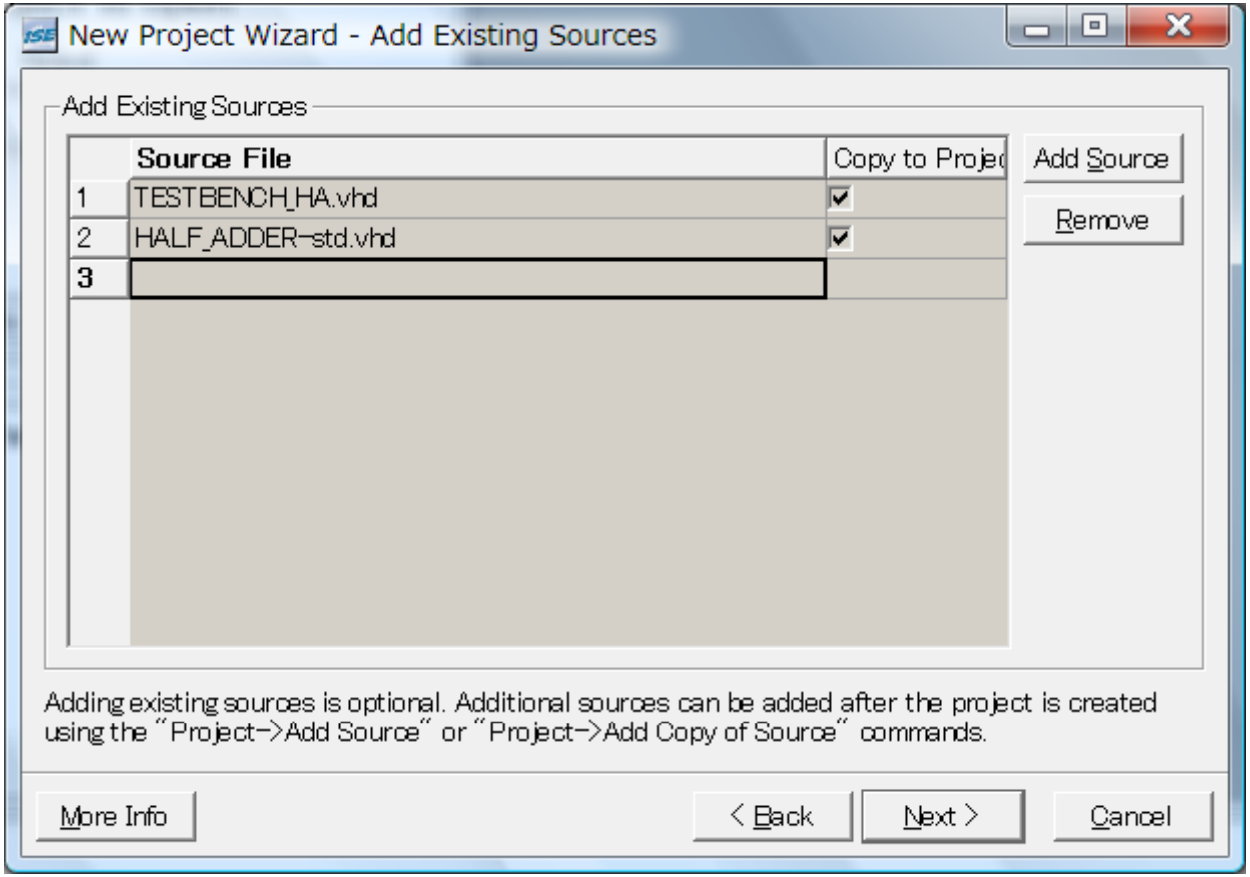
ここは設定なし


New Project Wizard - Device Properties
Select the Device and Design Flow for the Project
Property Name
Value
Product Category
All
Family
Automotive CoolRunner2
Device
Automatic xa2c000
Package
*
Speed
-*
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
ISE Simulator (VHDL/Verilog)
Enable Enhanced Design Summary
Enable Message Filtering
Display Incremental Messages
More Info
< Back
Next >
Cancel

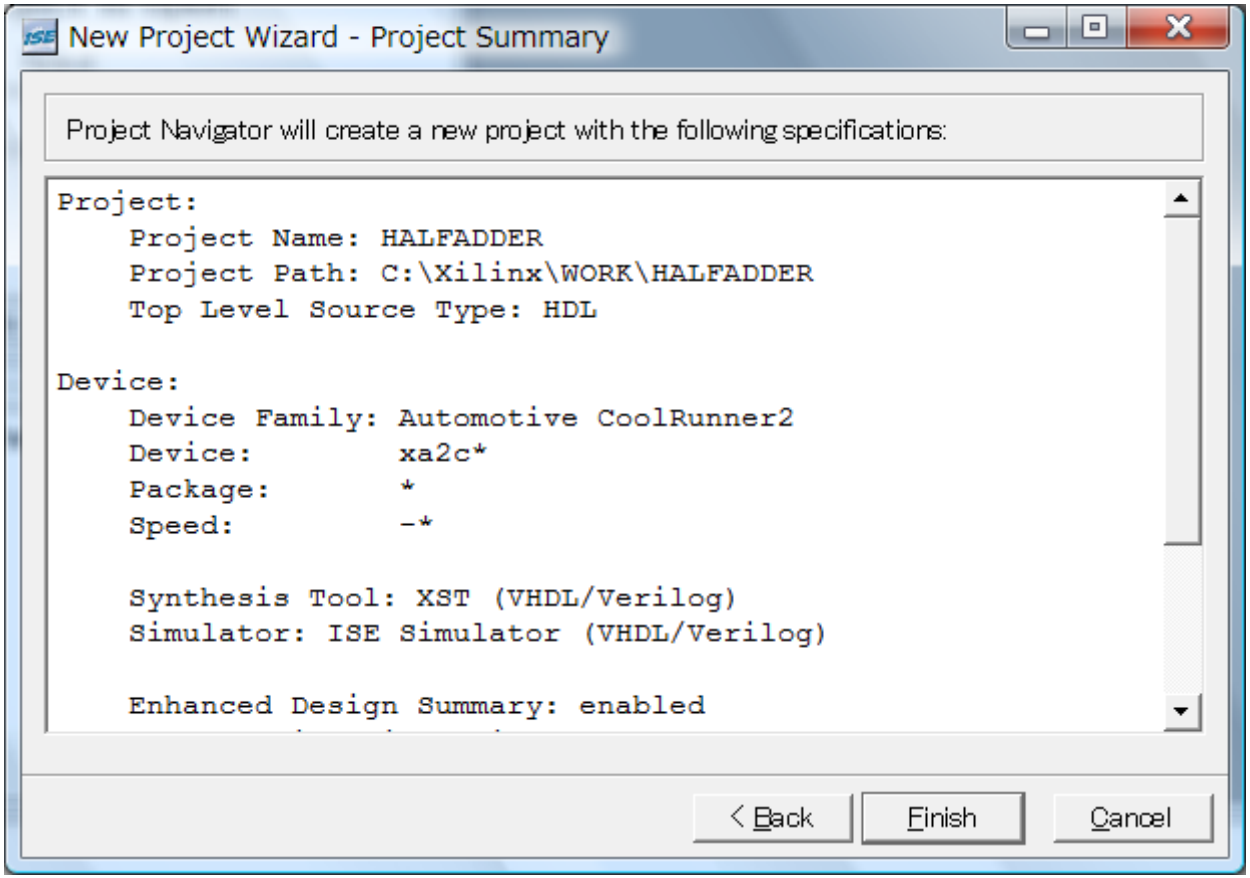
ここも、設定なし


New Project Wizard - Create New Source
Create a New Source
Source File
Type
1
New Source...
Remove
Creating a new source to add to the project is optional. Only one new source can be created with the New Project Wizard. Additional sources can be created and added to the project by using the "Project->New Source" command.
Existing sources can be added on the next page.
More Info
< Back
Next >
Cancel

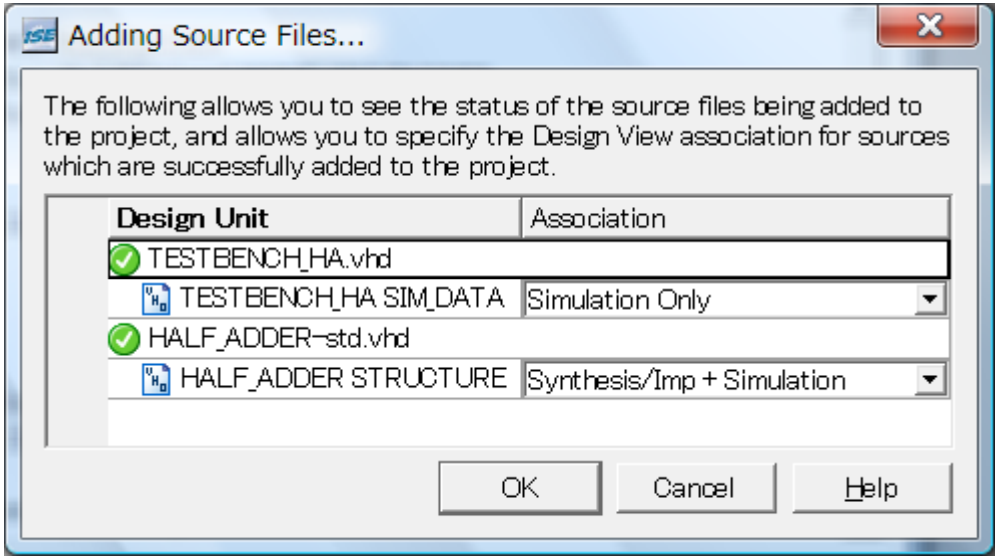
Add_Sourceで、
シミュレーションファイルを追加



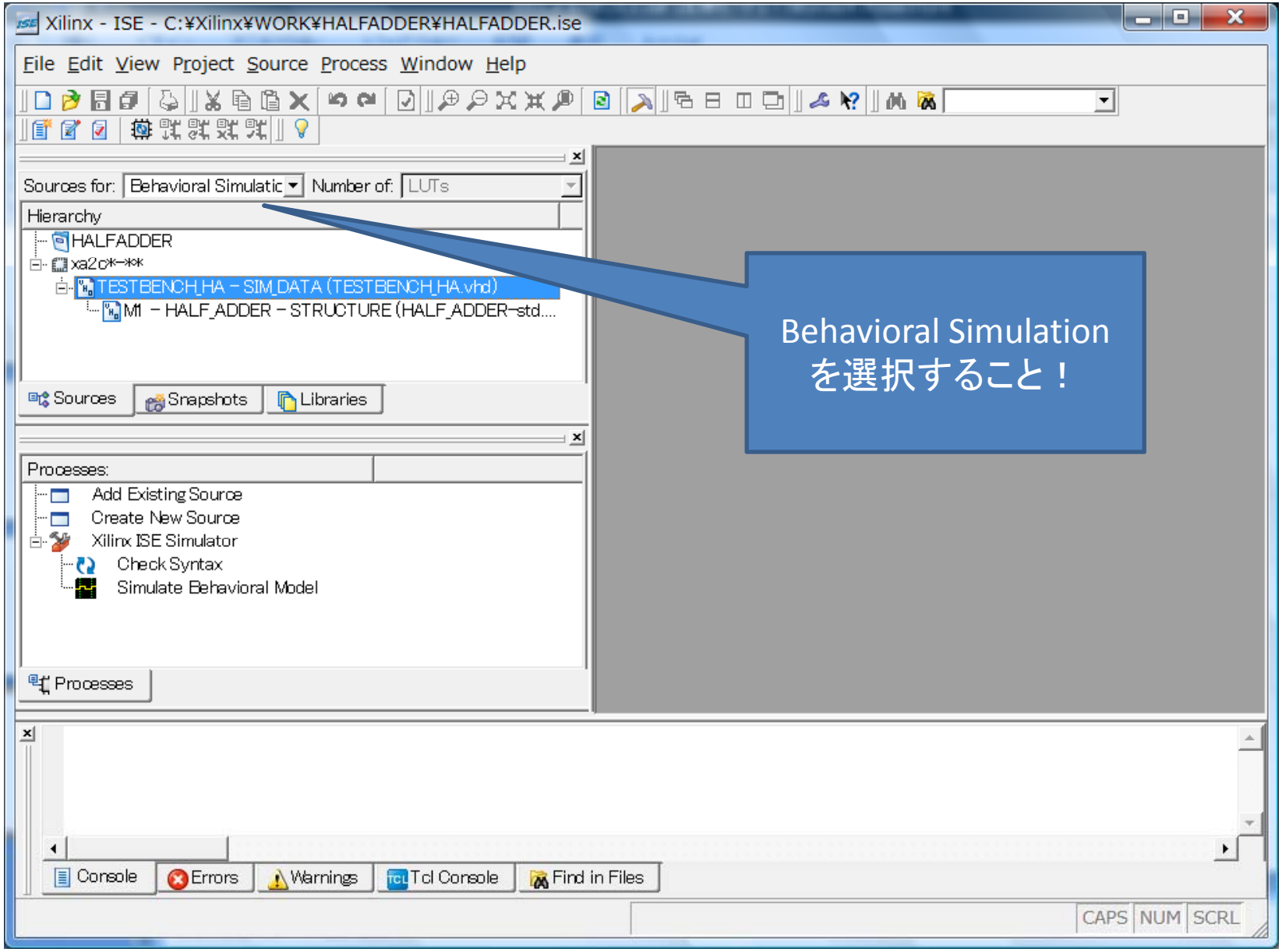
設定を確認し、Finish



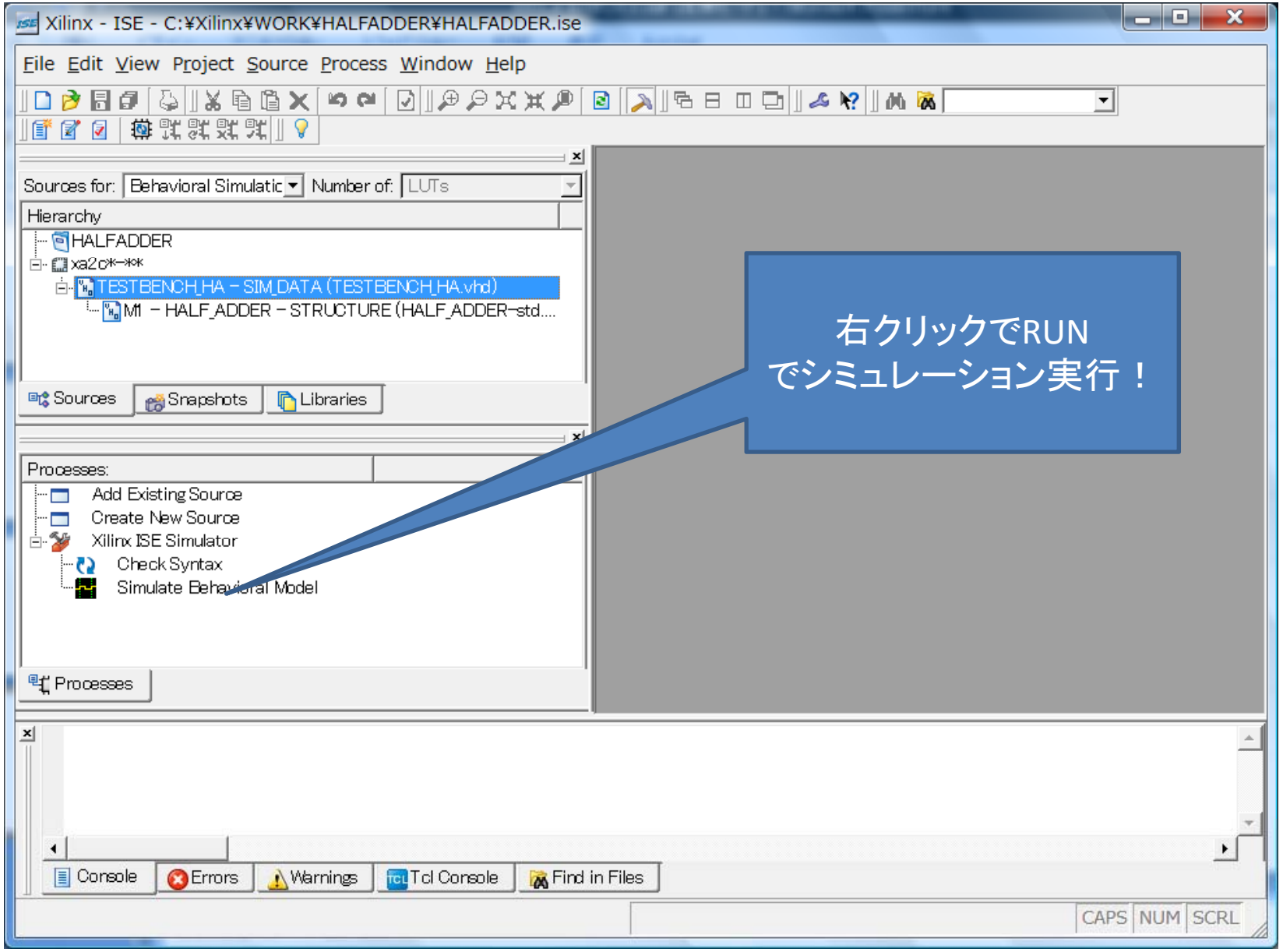
確認し、OK!


Adding Source Files...
The following allows you to see the status of the source files being added to the project, and allows you to specify the Design View association for sources which are successfully added to the project.
Design Unit
Association
TESTBENCH_HA.vhd
TESTBENCH_HA SIM_DATA
Simulation Only
HALF_ADDER-std.vhd
HALF_ADDER STRUCTURE
Synthesis/Imp + Simulation
OK
Cancel
Help

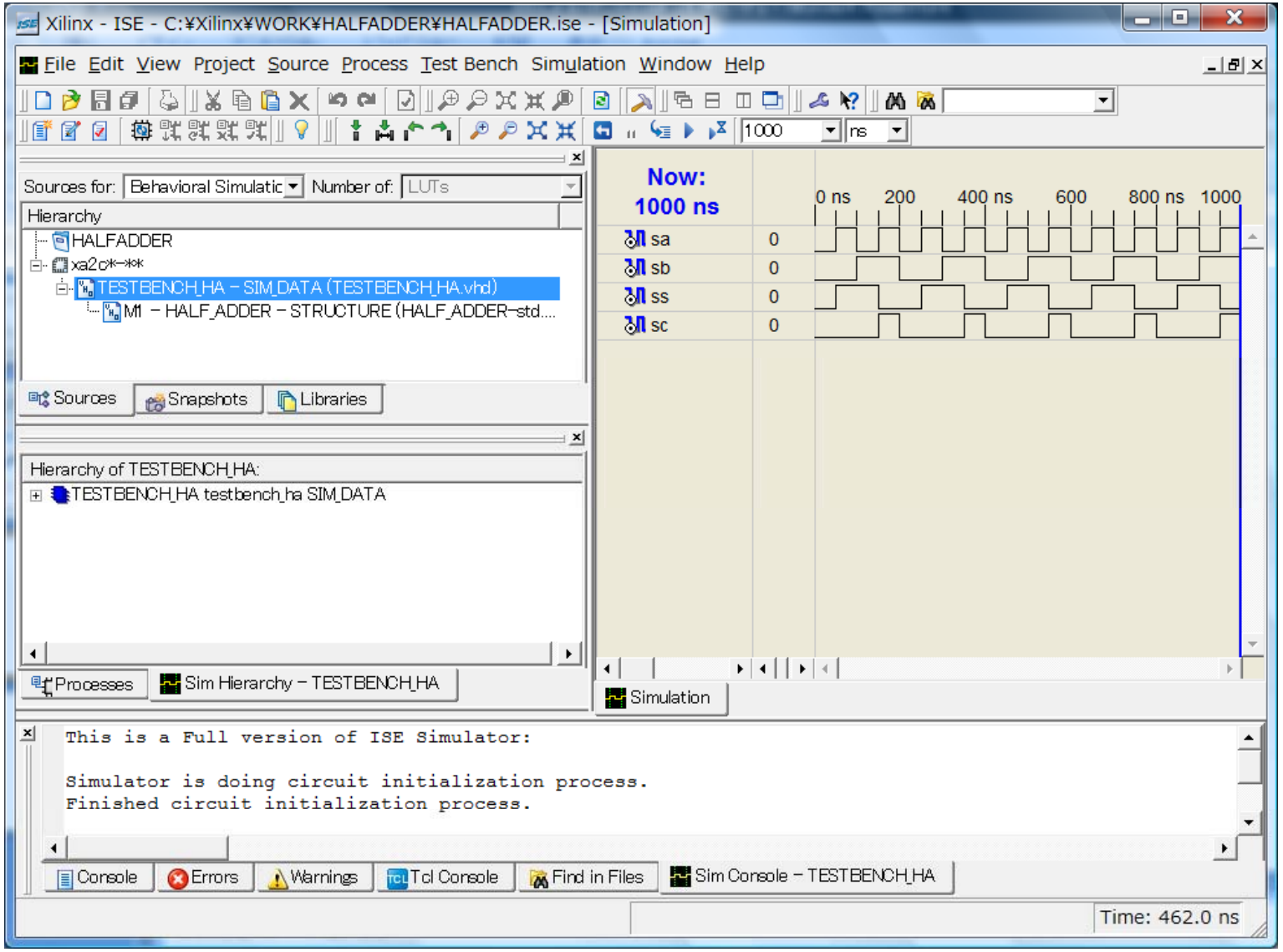
このようになればOK！


Xilinx - ISE - C:¥Xilinx¥WORK¥HALFADDER¥HALFADDER.ise
File Edit View Project Source Process Window Help
Sources for: Behavioral Simulatic
Number of: LUTs
Hierarchy
HALFADDER
xa2c*-**
TESTBENCH_HA - SIM_DATA (TESTBENCH_HA.vhd)
M1 - HALF_ADDER - STRUCTURE (HALF_ADDER-std....
Sources
Snapshots
Libraries
Processes:
Add Existing Source
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral Model
Processes
Behavioral Simulation
を選択すること！
Console
Errors
Warnings
Tcl Console
Find in Files
CAPS
NUM
SCRL

シミュレーション実行方法



シミュレーション実行され、
動作波形が表示されます！



アナウンス

- 次回　10/19はツール関連の指導をTAより実施予定
  - TA: ファイヤー和田研M2 宮野智法
  - tomo@lsi.ie.u-ryukyu.ac.jp

- 10/26はオンラインテスト（１回目）で、本日のデモに類することを各自のコンピュータでやってもらう予定です。