

Base System Builder wizard を選択して、[OK]をクリック。

Xilinx Platform Studio – no project opene	ed - [[Platform Studio]]	. 7 x
<u>File Edit View Project Hardware Software Dev</u>	ice Co <u>n</u> figuration <u>D</u> ebug Si <u>m</u> ulation <u>W</u> indow <u>H</u> elp	
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Project Information Area		<u>~</u>
Project Applications IP Catalog	Select desired text for more information	
	Documentation Examples Application Notes	
	Starting your project –O	
	Xilinx Platform Studio	
	Hardware Development	
	Begin by using the Base System Builder*	
	O Base System Builder wizard (recommended) Creating custom peripherals**	
	Blank XPS project	
	hardware design	
	Open a recent project Implementing your hardware platform	
	Browse for More Projects Simulating your embedded sub-system*	
	Debugging hardware using ChipScope Pro™∗	
	Browse installed EDK examples (projects) here	
	Downloading the complete system	
	Initializing FPGA on-chip memory with Mitting embedded software to a	~
[Platfo		
		~
		>
Output Warning Error		
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🗢 Create New XPS Project Using BSB Wizard 🛛 🛛 🔀
New project Project file Browse
Advanced options (optional: F1 for help)
Browse
OK Cancel

[Browse] をクリック

Platform Studio	Project			? 🛛
保存する場所①:	🗀 Lab	•	← 🗈 💣 🎟 -	
していた 最近使ったファイル	Complete Codoc Collab4			
デスクトップ	Callab1			
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र्च रे७१७-७				
	ファイル名(N): ファイルの種類(T):	system Platform Studio Project (*.xmp)	•	開((<u>(</u>)) キャンセル

作業用フォルダに 「lab1」という フォルダをつくって、 そこに保存!

🗢 Create New XPS Project Using BSB Wizard	×
New project Project file	
C:/fpga/Lab/lab1/system.xmp Browse)
Advanced options (optional: F1 for help)	5
Set Project Peripheral Repositories	
Browse	
OK Cancel	

ファイルの保存先を確認して [OK] をクリック

「I would like to create a new design」 を選択して [Next] をクリック

🔶 Base System Builder – Welcome Embedded Development Kit Platform Studio THINK Welcome to the Base System Builder! This tool will lead you through the steps necessary to create an embedded system. Please begin by selecting one of the following options: I would like to create a new design O I would like to load an existing .bsb settings file (saved from a previous session) Browse. <u>M</u>ore Info < <u>B</u>ack <u>N</u>ext > Cancel 💠 Base System Builder – Select Board

Select a target development board:

Select board

⊙ I would like to create a system for the following <u>d</u>evelopment board

¥

¥

Board vendor: Xilinx

Board name: Virtex 4 ML403 Evaluation Platform

Board revision: 1

Note: Visit the vendor website for additional board support materials.

Vendor's Website

Download Third Party Board Definition Files

O I would like to create a system for a custom board

Board description

The ML403 board is intended to showcase and demonstrate Virtex-4 technology, especially the new features being added to the FPGA. The ML403 board utilizes Xilinx Virtex 4 XC4VFX12-FF668 device. It is a demonstration platform to showcase the enormous power and flexibility of Virtex-4 FPGAs including new and improved clock technology, DSP blocks, Smart RAM blocks, advanced I/Os, embedded MACs, embedded processors, USB, and more.

Contact Info

More Info

「I would like to create a system for the following development board」 を選択し、

Board vendor : Xilinx Board name : Virtex 4 ML403 Evaluation Platform Board revision : 1

を選んで、[Next] をクリック

virtex4	<u>D</u> 01100	Fac <u>k</u> age.	Speed grade:	
	xc4vfx12	✓ ff668	-10	
	ping			
				た
lect the proces	ssor you would like	touse in this design:		
Processors				
MicroBlaze	•			
⊙ <u>P</u> owerPC				
Processor desc	ription			
The PowerPC	(R) 405 processor c	ore is a 32-bit impleme	ntation of a RISC Powe	rPC
and Virtex-4	FX device using the	IP-Immersion technolo	gy and supported by	
CoreConnect	bus infrastructure a	nd extensive IP cores f	or peripherals and utiliti	es.

[Processors] で 「Power PC」が選択されている か、確認して[Next]をクリック。

ここではなにも変えません。

00.00 MHz 100.00 MHz 5000 MHz nsure that your board is configured for the specifed frequency. eset polarity: Active LOW Image: Configuration Debug I/F Image: Configuration Image: Configuration Debug I/F Image: Configuration Image: Configuration OPU debug user pins only CPU debug and trace pins Image: Configuration Image: Configuration Image: Configuration Image: Configuration Image: Configuration	equency:	<u>P</u> rocessor ci frequency:	ock	Bus clock <u>f</u> requency:
nsure that your board is configured for the specified frequency. eset polarity: Active LOW cocessor configuration Debug I/F Orega _TAG CPU debug user pins only CPU debug and trace pins No debug On-chip memory (OCM) (Use BRAM) Data: NONE Instruction: NONE Instruction: NONE For optimal performance, enable burst and/or	00.00	MHz 100.00	MHz	50.00 V MHz
eset polarity: Active LOW ocessor configuration Debug I/F • FPGA JTAG • CPU debug user pins only • CPU debug and trace pins • No debug • On-chip memory (OCM) (Use BRAM) Data: NONE Pata: NONE Instruction: NONE For optimal performance, enable burst and/or	nsure that your t	poard is configured for	the specifed	frequency.
Debug I/F Image: Program of the	eset polarity:	Active LOW 🔽		
Debug I/F FPGA JTAG CPU debug user pins only CPU debug and trace pins No debug On-chip memory (OCM) (Use BRAM) Data: NONE Instruction: NONE Cache setup Enable For optimal performance, enable burst and/or	rocessor configu	ration		
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 CPU debug and trace pins No debug On-chip memory (OCM) (Use BRAM) Data: NONE Instruction: NONE Cache setup Enable For optimal performance, enable burst and/or 	O CPU debug	user pins only		
No debug On-chip memory (OCM) (Use BRAM) Data: NONE Instruction: Instruction: NONE For optimal performance, enable burst and/or	🔿 CPU debug	and trace pins		
Cache setup	🔘 No debu <u>e</u>			
	Cache setup	ormance, enable burst	and/or	(Use BRAM) <u>D</u> ata: NONE Instruction: NONE
	Enable floatin	g point unit (<u>F</u> PU) (?	

Reference clock : 100MHz Processor clock : 100MHz Bus clock : 50MHz

Debug I/F : FPGA JTAG OCM : NONE Cache : NONE

に設定して、[Next]をクリック

🎔 Base System Builder – Configur	e IV Interfaces (I of	3)
The following external memory and IO devi	ices were found on your boa	rd:
Xilinx Virtex 4 ML403 Evaluation Platform	Revision I	
Please select the IO devices which you we do devices	ould like to use:	
RS232_Uart		Data Sheet
LEDs_4Bit		Data Sheet
Peripheral: XPS GPIO	v	
Use interrupt		
LEDs_Positions		Data Sheet
Peripheral: XPS GPIO	×	
Use <u>i</u> nterrupt		
Push_Buttons_Position		Data Sheet
Peripheral: XPS GPIO	×	
Use <u>i</u> nterrupt		
More Info	K Back Next 2	Cancel

・LEDs_4Bit
(※[Use interrupt] に チェックを忘れないように!)
・LEDs_Positions
・Push_Buttons_Position

にチェックを入れて、 [Next]をクリック。

(他は使いませんので、チェックが 入っていたら外してください)

この部分のチェックは全部はずしてください。

The following external memory and IO devices w Xilinx Virtex 4 ML403 Evaluation Platform Revis Please select the IO devices which you would lik	vere found on your board: sion 1 ke to use:
	Data Sheet
SysACE_CompactFlash	Data Sheet
Cypress_USB	Data Sheet
DDR_SDRAM	Data Sheet
Ethernet_MAC	Data Sheet No <u>t</u> e
More Info	< <u>B</u> ack <u>N</u> ext > Cancel

TriMode MAC GMI	
	Data Sheet
SRAM	
	Data Sheet
	Data Sheet

Base System Builder - Add Internal Peripherals (Lot 1) Add other peripherals that do not interact with off-chip components. Use the "Add Peripheral" button to select from the list of available peripherals. If you do not wish to add any non-IO peripherals, click the "Next" button. Add Peripherals Peripherals rps_bram_if_onthr_1 Peripheral: XPS BRAM IF CNTLR Memory size: 8 KB	[Add Peripheral]をクリックし XPS_BRAM_IF_CNTLR
Add Peripheral Select the peripheral you want to add: XPS BRAM IF ONTLR OK Cancel	■ を選択し、[OK] をクリック。 (この作業を2回やります)
<u>More Info</u> < <u>B</u> ack <u>N</u> ext > Cancel	

🤝 Base System Builder – Add Internal Peripherals (1 of	D 🔽
Add other peripherals that do not interact with off-chip components. L "Add Peripheral" button to select from the list of available peripherals.	lse the
If you do not wish to add any non-IO peripherals, click the Next butt	on. <u>A</u> dd Peripheral
- Peripherals	
xps_bram_if_cntlr_1 Peripheral: XPS BRAM IF CNTLR	<u>R</u> emove
Memory <u>s</u> ize: 64 KB 💌	Data Sheet
xps_bram_if_ontlr_2 Peripheral: XPS BRAM IF CNTLR	Remove
Memory <u>s</u> ize: <u>4 KB</u>	Data Sheet
xps_bram_if_cntlr_3	Remove
Memory size: 4 KB	Data Sheet
More Info	Cancel

xps_bram_if_cntlr_1 64KB xps_bram_if_cntlr_2 4KB xps_bram_if_cntlr_3 4KB

に設定し、[Next] をクリック

🖤 Base System Builder – Software Setup

Devices to use	as standard input, standard output, and b	oot memory
STD <u>I</u> N:	None	~
STD <u>O</u> UT:	None	~
<u>B</u> oot Memory:	xps_bram_if_cntlr_1	~

-Sample application selection

Select the sample C application that you would like to have generated. Each application will include a linker script.

Memory <u>t</u>est

Illustrate system aliveness and perform a basic read/write test to each memory in your system

Peripheral selftest

Perform a simple self-test for each peripheral in your system.

Below are other software applications found for your board. In order to select an application, please ensure your system satisfy the requirements. See "More Details".

ML403 Cypress USB Application

More Details...

[Sample application] は 「Peripheral selftest」のみを 選択し、[Next] をクリック。

他はなにも触りません。

💖 Base System Builder – Configure Peripheral Test Application 👘

The Peripheral Selftest application includes a simple self test for each periperhal in your system (if such a selftest function exists in the driver the peripheral).

-PeripheralTest

Select the memory devices which will be used to hold the following program sections:

Instruction:	xps_bram_if_cntlr_1	×
<u>D</u> ata:	xps_bram_if_cntlr_1	~
<u>S</u> tack/Heap:	xps_bram_if_cntlr_1	*

PowerPC interrupt vector must be starting at 64KB boundary, so not all memories can be used for the interrupt vector.

~

Interrupt <u>V</u> ec:	xps_bram_if_cntlr_1
------------------------	---------------------

WARNING -

Due to the expected size of this application, it is highly recommended that you place the Instruction and Data sections in an external memory. You will have to use a debugger, bootloader, or ACE file to initialize the memory.

「Instruction」,「Data」, 「Stack/Heap」は全て

xps_bram_if_cntlr_1

に格納されてるか確認して、 [Next] をクリック

More Info	< <u>B</u> ack <u>N</u> ext >	Cancel

💖 Base System Builder – System Greated

Below is a summary of the system you have created. Please review the information below. If it is correct, hit Generate> to enter the information into the XPS data base and generate the system files. Otherwise return to the previous page to make corrections.

Processor: ppc405_0 Processor clock frequency: 100.00 MHz Bus clock frequency: 50.00 MHz On Chip Memory : 72 KB

The address maps below have been automatically assigned. You can modify them using the editing features of XPS.

PLB Bus : PLB_V4	6 Inst. name: plb	Attached Components:			
Core Name	Instance Name	Base Addr	High Addr		
xps_bram_if_cntlr	xps_bram_if_cntlr_1	0×FFFF0000	0×FFFFFFFF		
xps_gpio	LEDs_4Bit	0×81400000	0×8140FFFF		
xps_gpio	LEDs_Positions	0×81420000	0x8142FFFF		
xps_gpio	Push_Buttons_Position	0×81440000	0×8144FFFF		
xps_bram_if_cntlr	xps_bram_if_cntlr_2	0×00000000	0×00000FFF		
xps_bram_if_cntlr	xps_bram_if_cntlr_3	0×FFFE8000	0×FFFE8FFF		
xps_intc	xps_intc_0	0×81800000	0x8180FFFF		

<u>M</u> ore Info	< Back Generate Cancel

[Generate] -> [Finish] をクリック。 これで最初の設定は終わりです。



メニューの [Hardware] から [Generate Bitstream]を実行(しばらく時間がかかります)

🔶 Xilinx Platform Studio –	C:/fpga/Lab/lab1/system.xm	ip – [System Assembly Vi	iew1]			_ ₽ 🛛
<u>File E</u> dit <u>V</u> iew <u>P</u> roject <u>Har</u> d	ware <u>S</u> oftware Device Co <u>n</u> figurati	on <u>D</u> ebug Si <u>m</u> ulation <u>W</u> indow	<u>H</u> elp			
8 🗅 🖻 🖥 🕹 8 🖬 🕷	Generate <u>N</u> etlist	🖉 😼 🖸 这 🗄 👪 📓 🏀	🜌 🗠 📥 🔃 🏫 🖽	『 船 🗄 🐹 淡	🖻 🕅 X X 🍡 🗏 🔟 🖵 😽	
Project Information Area	Generate <u>B</u> itstream	Bus Interfaces Ports	Addresses			SIF Filters
Project Applications I 🌺	Create or Import Peripheral	Name	Bus Connection	IP Type	IP Version	
Platform 🕅	Configure <u>C</u> oprocessor			ppc405_virtex4	2.01.a	
😑 Project Files	Check and View Core Licenses	> plb		plb_v46	1.02.a	
MHS File: system.mhs	Olean Netlist	🗟 🗢 xps_bram_if_cntlr_1		xps_bram_if_cntlr	1.00.a	
MSS File: system.mss 🦉	Olean Netlist	₽		xps_bram_if_cntlr	1.00.a	
MBACT Command Filett	Clean Bits	· · · · · · · · · · · · · · · · · · ·		xps_bram_if_cntir	1.00.a	
Implementation Option	Clean Hardware	pip_bram_if_cntir_i_bram for the second se		bram_block	1.00.a	
Bitgen Options File: etc/bit	renut	Solution of the second seco		bram block	1.00.a	
Project Options				jtagppc ontlr	2.01.a	
Device: xc4vfx12ff668-10		⊕ → proc_sys_reset_0		proc_sys_reset	2.00.a	
Netlist: TopLevel	· · · 🎍	⊕- ◆ LEDs_4Bit		xps_gpio	1.00.a	
Implementation: XPS (Xflow)	u 🔰	🕞 🗢 LEDs_Pasitians		xps_gpio	1.00.a	
HDL: VHDL	• •	🔒 🗢 Push_Buttons_Position		xps_gpio	1.00.a	
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メニューの [Software] から 「Generate Libraries and BSPs」を実行

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ject Applications IP Catalog	Assign Default <u>D</u> rivers		Bus Connectio	n IP Type	IP Version		
form	ueg Generate Libraries and	BSPs 50		ppc405_virtex4	2.01.a		
roject Files	En Add Software Applicat	ion Project		plb_v46	1.02.a		
MHS File:system.mhs		ion Project am_if_cntlr_	1	xps_bram_if_cntlr	1.00.a		
MSS File: system.mss	Build All User Applicat	tions am_if_cntlr	2	xps_bram_if_cntlr	1.00.a		
	Get <u>P</u> rogram Size	am_if_cntlr	3	xps_bram_if_cntlr	1.00.a		
iMPACT Command File: etc/dowr	r 🛐 <u>G</u> enerate Linker Script		1_bram	bram_block	1.00.a		
-Implementation Options File: etc/	U ^b G. Clean Libraries	am_if_cntlr	2_bram	bram_block	1.00.a		
Bitgen Options File: etc/bitgen.ut		am_if_ontlr	3_bram	bram_block	1.00.a		
roject Options	nean Programs	c_0		jtagppc_cntlr	2.01.a		
Device: xc4vtx12tt668-10	🤰 Clean Software	ys_reset_0		proc_sys_reset	2.00.a		
Netlist: TopLevel		ABR		xps_gpio	1.00.a		
uni vuni		Duck Rutters Des		xps_gpio	1.00.a		
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Reference Files		└─� <i>clack_generator_</i> 0	,	clock_generator	200.a		
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Keterence Files ⊕ Log Files ⊕ Synthesis Report Files	[Platform Studio]	System Assembly View	Block Diagram	clock_generator	200.a		
Reference Files Log Files Synthesis Report Files Compiling common	[Platform Studio]	System Assembly View	Block Diagram	clock_generator	200.a		
Reference Files Tog Files Synthesis Report Files Compiling common	(Platform Studio)	System Assembly View	Block Diagram	clock_generator	200.a		~
Reference Files Tog Files Synthesis Report Files Compiling common Libraries generated in	Platform Studio] C:\fpga\Lab\lab1\	System Assembly View	Block Diagram	clock_generator	200.a		
Reference Files Dog Files Synthesis Report Files Compiling common Libraries generated in Running execs_generate	Platform Studio] 1 C:\fpga\Lab\lab1\ ter of of of the state of the studio]	System Assembly View ppc405_0\lib\ directions and Libraries	Block Diagram	clock_generator	200.a		<u> </u>
Reference Files Description: Log Files Compiling common Libraries generated in Running execs_generate LibGen Done. Done!	<pre>> [Platform Studio] 1 C:\fpga\Lab\lab1\ 2 for O5'es, Driver</pre>	System Assembly View	Block Diagram	clock_generator	200.a		
Keterence Files	Platform Studio] C:\fpga\Lab\lab1\ for O5'es, Driver	System Assembly View ppc405_0\lib\ dire	Block Diagram	clock_generator	200.a		
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メニューの [Device Configuration] から Update Bitstreamを実行

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<u>File Edit View Project Hardware Softwa</u>	are Device Co <u>n</u> figuration	on <u>D</u> ebug Si <u>m</u> ulation <u>W</u>	(indow <u>H</u> elp				
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Project Applications IP Catalog	Program Flash	n Memory	Bus Connection	IP Type	IP Version		
'latform		<u>⊕</u> - ∞ ppc405_0		ppc405_virtex4	2.01.a		
Project Files	117			plb_v46	1.02.a		
MHS File:system.mhs		🚊 🗢 xps_bram_if_cntlr_1		xps_bram_if_cntlr	1.00.a		
MSS File: system.mss		💼 🗢 xps_bram_if_cntlr_2		xps_bram_if_cntlr	1.00.a		
UCF File: data/system.ucf		🕀 🗢 xps_bram_if_cntlr_3		xps_bram_if_cntlr	1.00.a		
		⊕ ◇ plb_bram_if_cntlr_1_	bram	bram_block	1.00.a		
Implementation Options File: etc/fast_ri	Þ + Þ+++	🕀 🗢 xps_bram_if_cntlr_2	bram	bram_block	1.00.a		
Bitgen Options File: etc/bitgen.ut		⊕ ◇ xps_bram_if_cntlr_3	bram	bram_block	1.00.a		
Project Uptions		I → itagppc_U		jtagppc_cntir	2.01.a		
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Beference Files		clack severator 0		clock generator	200 a		
in log Files				olook_gonorator	2.00.0		
	[Platform Studio]	System Assembly View	Block Diagram				
Cutout Warning From							

メニューの [Device Configuration] から 「Download Bitstream」を実行



ボード右下のLEDが点灯するかどうか確認してください! "CPU Reset"のプッシュボタンで再動作できます。