SYSTEM ARCHITECTURE
ADVANCED SYSTEM ARCHITECTURE
Graduate School of Engineering and Science, Univ. of the Ryukyus

2013/Fall-Winter Term
Monday 12:50

Room# 1-322 or 5F Meeting Room

Instructor: Fire Tom Wada, Professor

Course Description

- This course focuses wireless communication system.
- Lecture Plan

1.	Background & Mathematics	Bateman Chap.1
2.	Introduction of Data transmission	Bateman Chap.2
3.	Doppler Shift & Wireless channel	Bateman Chap.4
4.	Digital Modulation (1)	Bateman Chap.5
5.	Digital Modulation (2)	Bateman Chap.6
6.	Coding	Bateman Chap.7
7.	Multi User Access	Bateman Chap.8
8.	OFDM system	Luo Chap.18
9.	Matlab Lab	
10.	Student project and presentations	

Notes

- Two books copy will be distributed.
  1. Digital Communications –Designs for real World-, Andy Bateman
  2. Digital Front-End in Wireless Communications and Broadcasting, edited by Luo
     Chapter 18 by Tomohisa Wada
- Grading:
  - Small Presentation (20%)+Midterm Lab report (40%) + Final project presentation (40%)
- Digital signal processing simulation tool MATLAB will be used in the course or home works.

Information

- Tomohisa Wada, (Fire Tom Wada)
- Email: wada@ie.u-ryukyu.ac.jp
- Mobile Phone: 090-9785-5802
- Office: 1-605
- URL: http://www.ie.u-ryukyu.ac.jp/~wada/lecture.html
  - **MATERIALS WILL BE AVAILABLE ON THE WEB**
- Office hour: Monday 15-16, Friday 11-12PM
  Please make reservation by email.

Self introduction -School-

- 1983/March
  - **BS degree from Osaka Univ. Electronic Engineering, JAPAN**
- 1992/January
  - **MS degree from Stanford Univ. Electrical Engineering, USA**
  - **Major: COMPUTER HARDWARE**
- 1994/December
  - **PhD from Osaka University, JAPAN**
  - **High Speed SRAM design methodologies and It's application to Cache memory**

Self introduction -Jobs (1)-

- 1983/4-1990/7
  - **Designer at Mitsubishi Electric LSI research Laboratories**
- 1990/7-1992/1
  - **Stanford University Electrical Engineering Master course**
  - Major: computer H/W, RISC
  - Computer Cache memory design
- 1992/1-1995/12
  - **Cache design project leader in Mitsubishi Electric for INTEL corporation**
- 1995/1-1996/5
  - **Design member for 3D Graphics rendering ASIC jointly developed by Mitsubishi Electric & Evans&Sutherland, UTAH**

Self introduction -Jobs (2)-

- 1996/6-1997/7
  - **Design member for Flash memory**
  - **Design member for low voltage SRAM (mobile application)**
- 1997/7-1999/4
  - **300MHz pipelined burst cache SRAM design team leader for INTEL pentium III**
- 1999/5
  - **Associate Professor at the Univ. of the Ryukyus, SOC design**
- 2001/4
  - **Professor at the University of the Ryukyus**
- 2001/3
  - **Founder of Magna Design Net, Inc at Naha**
  - **Fabless Broadband communication LSI venture company**

Student Self-introduction in Speech

1. Name,
2. Where are you from?
3. Master or Doctor, Grade, or Bachelor
4. Who is your supervisor?
5. What is your major , research topic?
6. Free talk.

Registration of the course

- Web registration
- Physical registration

Code	Course	webcode
R0040900	システムアーキテクチャ論	
R0046400	System Architecture	
R0078800	システムアーキテクチャ特論	
R0085400	Advanced System Architecture	

Lecture Sedule

- 1) 10/7 (mon)
- 2) 10/16 (wed)
- 3) 10/28 (mon)
- 4) 11/6 (wed)
- 5) 11/18 (mon)
- 6) 11/25 (mon)
- 7) 12/2 (mon)
- 8) 12/16 (mon)
- 9) 12/24 (mon)
- 10) 12/26 (thur)
- 11) 1/6 (mon)
- 12) 1/20 (mon)
- 13) 1/27 (mon)
- LAB) Saturday Matlab Lab will be held on Decemeber 21th maybe..

Note

- Next lecture: Oct. 29th
- Materials will be prepare on web, please make your printing copy before joining the lecture.
  - http://www.ie.u-ryukyu.ac.jp/~wada/lecture.html