

VLSI設計

-最初のML403ボード利用-

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IE dept.

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ML403ボードの接続

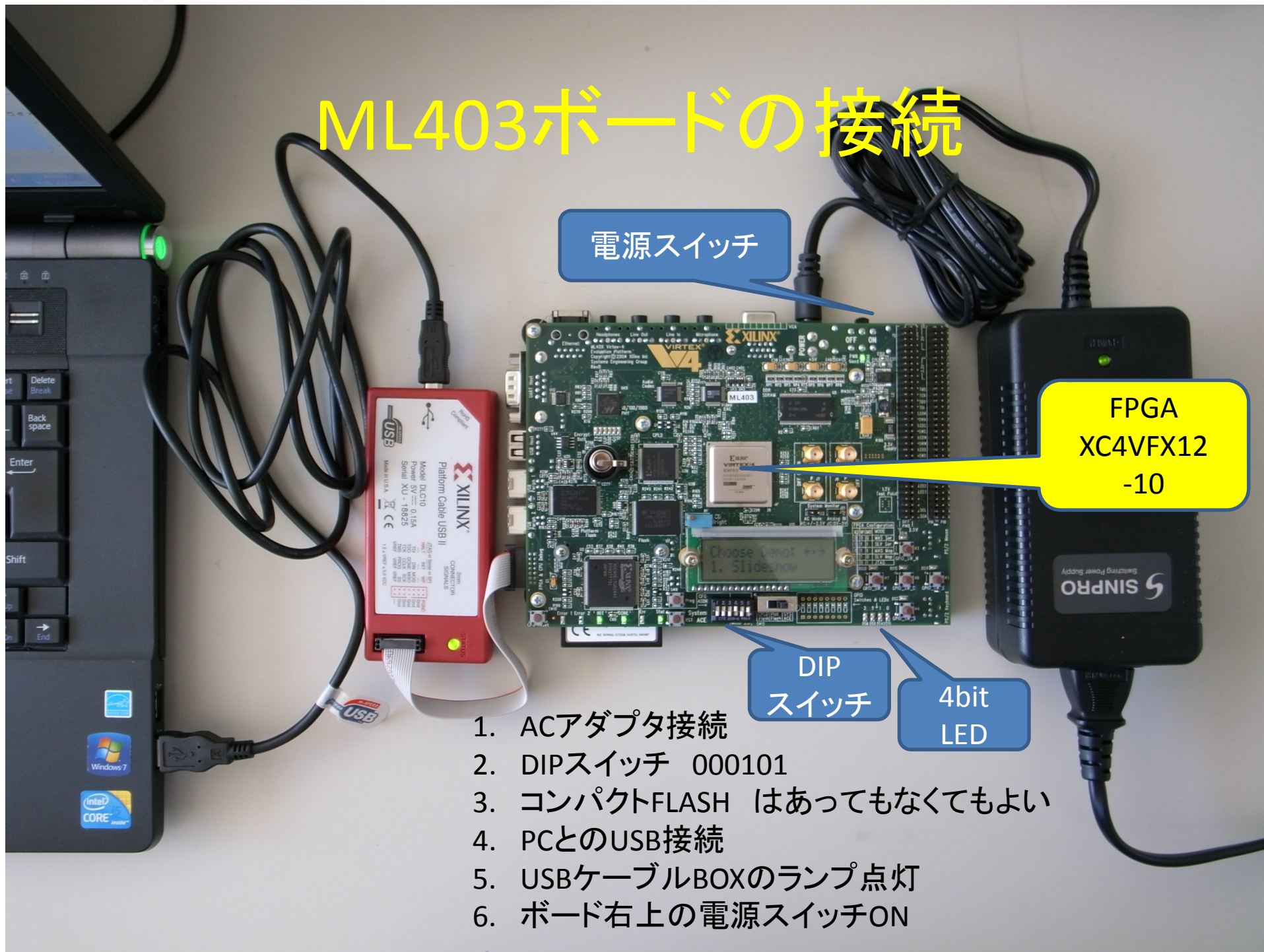
電源スイッチ

FPGA
XC4VFX12
-10

DIP
スイッチ

4bit
LED

1. ACアダプタ接続
2. DIPスイッチ 000101
3. コンパクトFLASH はあってもなくてもよい
4. PCとのUSB接続
5. USBケーブルBOXのランプ点灯
6. ボード右上の電源スイッチON



FPGA内にカウンターを作りLEDを点滅させる(1)

ツールを立ち上げ、必要なファイルを加える

1. Xilinx ISE Project Navigator起動
2. File -> New Project %新しい設計プロジェクトを作る
3. プロジェクト名を入力 new00
4. FPGAパラメータ等入力
 - Virtex4
 - XC4VFX12
 - FF668
 - -10
5. Finish %プロジェクトが完成
6. Project-> Add copy of sourceで以下の3つのファイルを加える
 - counter.vhd Association = ALL %シミュレーションにもFPGAにも使用
 - test_counter.vhd Association = Simulation %シミュレーションじのみ用
 - System.ucf Association = Implementation %FPGA生成時のみ使用

プロジェクト名入力

The screenshot displays the ISE Project Navigator application window. The main window shows a 'Welcome to the ISE® Design Suite' message and a 'New Project...' button. A 'New Project Wizard' dialog box is open, titled 'Create New Project'. The dialog prompts the user to 'Specify project location and type' and 'Enter a name, locations, and comment for the project'. The 'Name' field contains 'new00', the 'Location' and 'Working Directory' fields contain 'C:\%Ilinx%\work%new00', and the 'Top-level source type' dropdown is set to 'HDL'. The 'Description' field is empty. At the bottom of the dialog are 'More Info', 'Next', and 'Cancel' buttons. The background shows the ISE Project Navigator interface with a slide pane on the left and a console at the bottom. The system tray at the bottom right shows the date and time as 11:19 on 平成 23/10/6.

ISE Project Navigator (M.70d)

File Edit View Project Source Process Tools Window Layout Help

Start

Welcome to the ISE® Design Suite

Project commands

Open Project... Project Browser...
New Project... Open Example...

Recent projects

Double click on a project in the list below to open it

new1
dctALL1
mult

Additional resources

[ISE Design Suite InfoCenter](#)
[Key New Features in Project Navigator](#)
[Tutorials on the Web](#)
[Design Resources](#)

Console

Console Errors Warnings Find in Files Results

More Info Next Cancel

Specify project location and type.

Enter a name, locations, and comment for the project

Name: new00
Location: C:\%Ilinx%\work%new00
Working Directory: C:\%Ilinx%\work%new00
Description:

Select the type of top-level source for the project

Top-level source type:
HDL

クリックしてノートを入力

スライド 4/4 "Office テーマ" 日本語 (日本) 61% 11:19 平成 23/10/6

Project-> Add copy of sourceで 3つのファイルを加えた後

The screenshot shows the Xilinx ISE Project Navigator interface. The main window displays the 'Design Summary' for a project named 'test_counter'. The summary includes the following information:

test_counter Project Status			
Project File:	new00.xise	Parser Errors:	No Errors
Module Name:	test_counter	Implementation State:	New
Target Device:	xc4vfx12-10ff668	• Errors:	
Product Version:	ISE 12.3	• Warnings:	
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:		• Final Timing Score:	

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report					
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					

The console window at the bottom shows the following messages:

```
INFO:HDLCompiler:1061 - Parsing VHDL file "C:/Xilinx/work/new00/counter.vhd" into library work
INFO:ProjectMgmt:656 - Parsing design hierarchy completed successfully.
```

FPGA内にカウンタを作りLEDを点滅させる(2)

動作シミュレーション

1. Designウインドウの Simulationボタンを押す %シミュレーションモード
2. test_counter - behavior (test_counter.vhd)を選択する
 - テストベンチを選択しないとシミュレーションできません 注意です
3. ISim Simulatorをクリックし、Simulate Behavioral Modelをダブルクリック
 - %シミュレーション開始
4. Isimツールで
 1. Simulation->Run all で実行
 2. Simulation ->Breakでストップ
 3. View -> Zoom -> In やOutで拡大縮小
5. シミュレーションで動作を確認
6. Isimを終了

Isim実行 350msまでの結果

The screenshot displays the ISim (ModelSim) interface. The main window shows a waveform for the test_counter.vhd simulation. The waveform includes signals for sysclk, reset, output[3:0], and sysclk_period. The simulation is stopped at 337.730629651 ms. The console window shows the simulation process and the command '# run all'.

Name	Value
sysclk	1
reset	1
output[3:0]	0010
sysclk_period	10000 ps

Console output:

```
Simulator is doing circuit initialization process.  
Finished circuit initialization process.  
ISim>  
# run all  
Stopped at time : 371 091 660 ns : File "C:/Xilinx/work/new00/test_counter.vhd" Line 73  
ISim>
```

Sim Time: 371,091,660,000 ps

FPGA内にカウンターを作りLEDを点滅させる(3)

VHDL記述から回路を生成し、FPGAに転送

1. Designウインドウの Implementationボタンを押す %FPGA制作モード
2. 下側ウインドウのGenerate Programming Fileをダブルクリック
 - 回路を合成し、FPGA内部に配置し配線するので、時間かかる
 - Process "Generate Programming File" completed successfullyができればデータ完成
3. Tools -> iMPACT起動
4. ISE iMPACTで edit -> Launch wizard
 - Automatically connect to a cable and identify Boundary-Scan chainを選択し、OK
 - その後、no, cancelで次ページの図がでる。
 - 図のFPGAで右クリック Assign new configuration fileでcounter.bitを設定
 - 図のFPGAで右クリック ProgramでFPGAにデータを流し込む
5. ボード右下のLEDが点滅する。

ML403ボード上のJTAGの接続図

The screenshot displays the ISE iMPACT software interface during a Boundary Scan operation. The main window shows a diagram of the JTAG chain with four Xilinx components connected in series between TDI and TDO. A yellow callout bubble points to the third component, labeled 'FPGA XC4VFX12 -10'. Below the diagram, a blue box contains the text 'Identify Succeeded'. The console window at the bottom shows the following output:

```
PROGRESS_END - End Operation.  
Elapsed time = 1 sec.  
011
```

The status bar at the bottom of the software window indicates 'Configuration Platform Cable USB II 6 MHz usb-hs'. The Windows taskbar at the bottom shows the system time as 12:26 on 平成 23/10/6.

プログラム用ビットファイルが表示

The screenshot displays the ISE Project Navigator interface. The main window is titled "ISE iMPACT (M.70d) - [Boundary Scan]". The "IMPACT Flows" pane on the left shows a tree view with "Boundary Scan" expanded, containing "SystemACE", "Create PROM File (PROM ...)", and "WebTalk Data". The "IMPACT Processes" pane shows "Available Operations are:" with "Get Device ID", "Get Device Signature/Usercode", and "Read Device Status". The central diagram shows a Boundary Scan chain with four devices: "xc95144xl bypass", "xc4vfx12 counter.bit", "xc32p bypass", and "xc95144xl bypass". A yellow callout bubble points to the "xc4vfx12 counter.bit" device with the text "Bitファイル". The "Console" pane at the bottom shows "011". The status bar at the bottom indicates "Configuration Platform Cable USB II 6 MHz usb-hs". The Windows taskbar at the bottom shows the time as 12:32 on 平成 23/10/6.

LEDが点滅する



ボード上の部品の接続

